



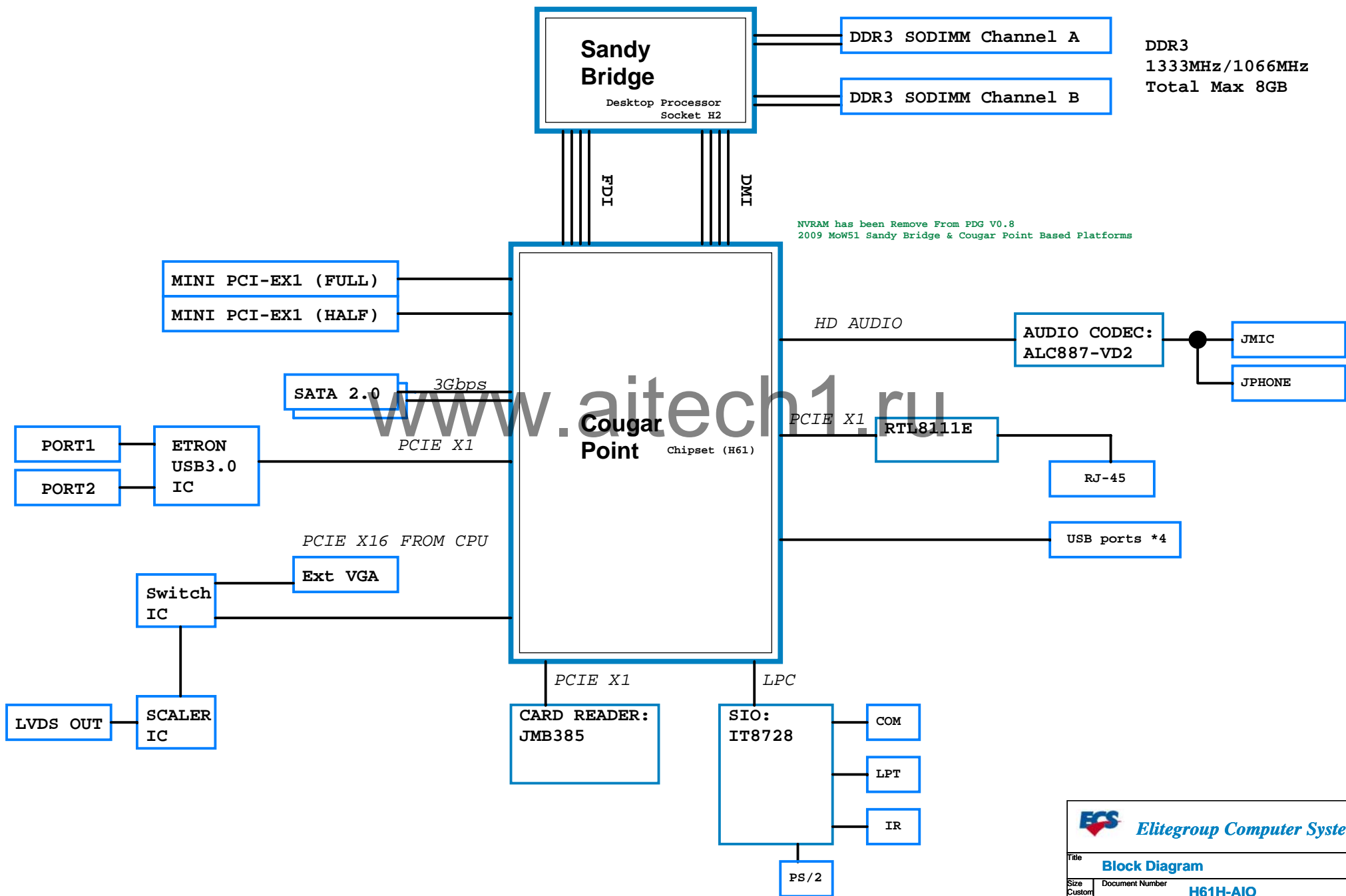
Acer fShenzhen AIO

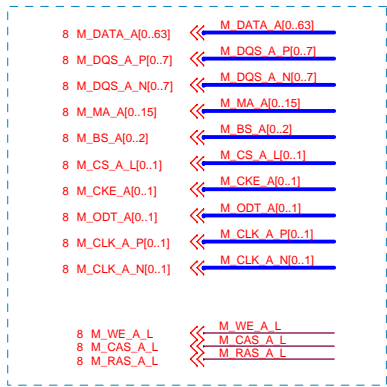
TABLE OF CONTENTS

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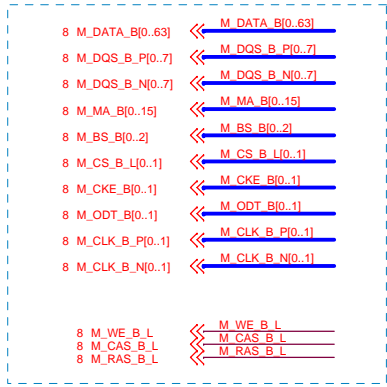
Rev : 1.0

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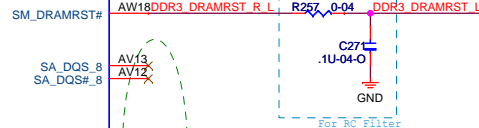
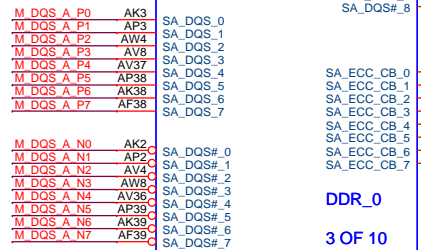
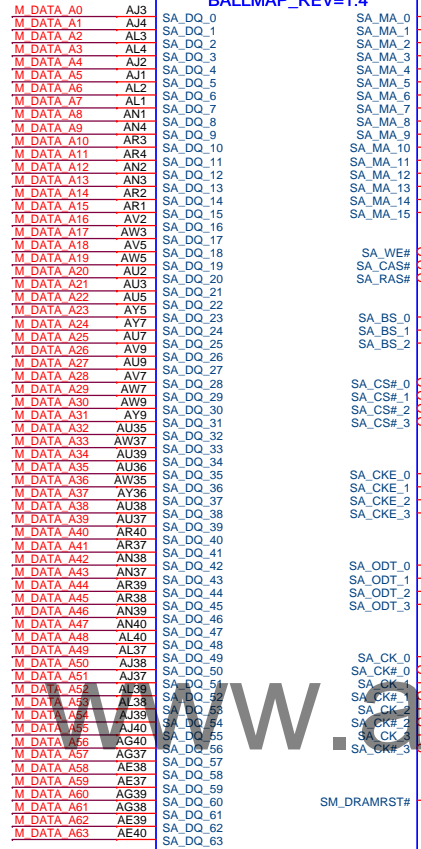




DDR3 CH.A

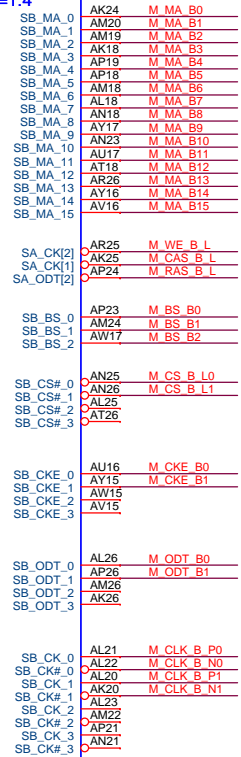
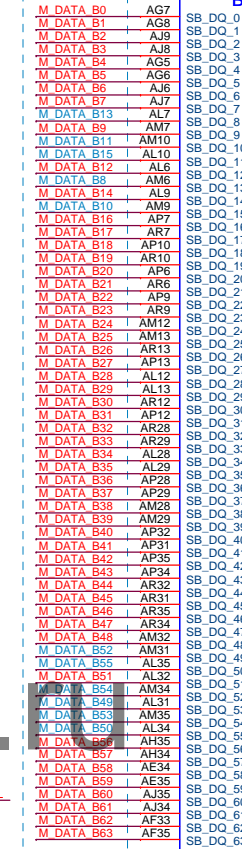


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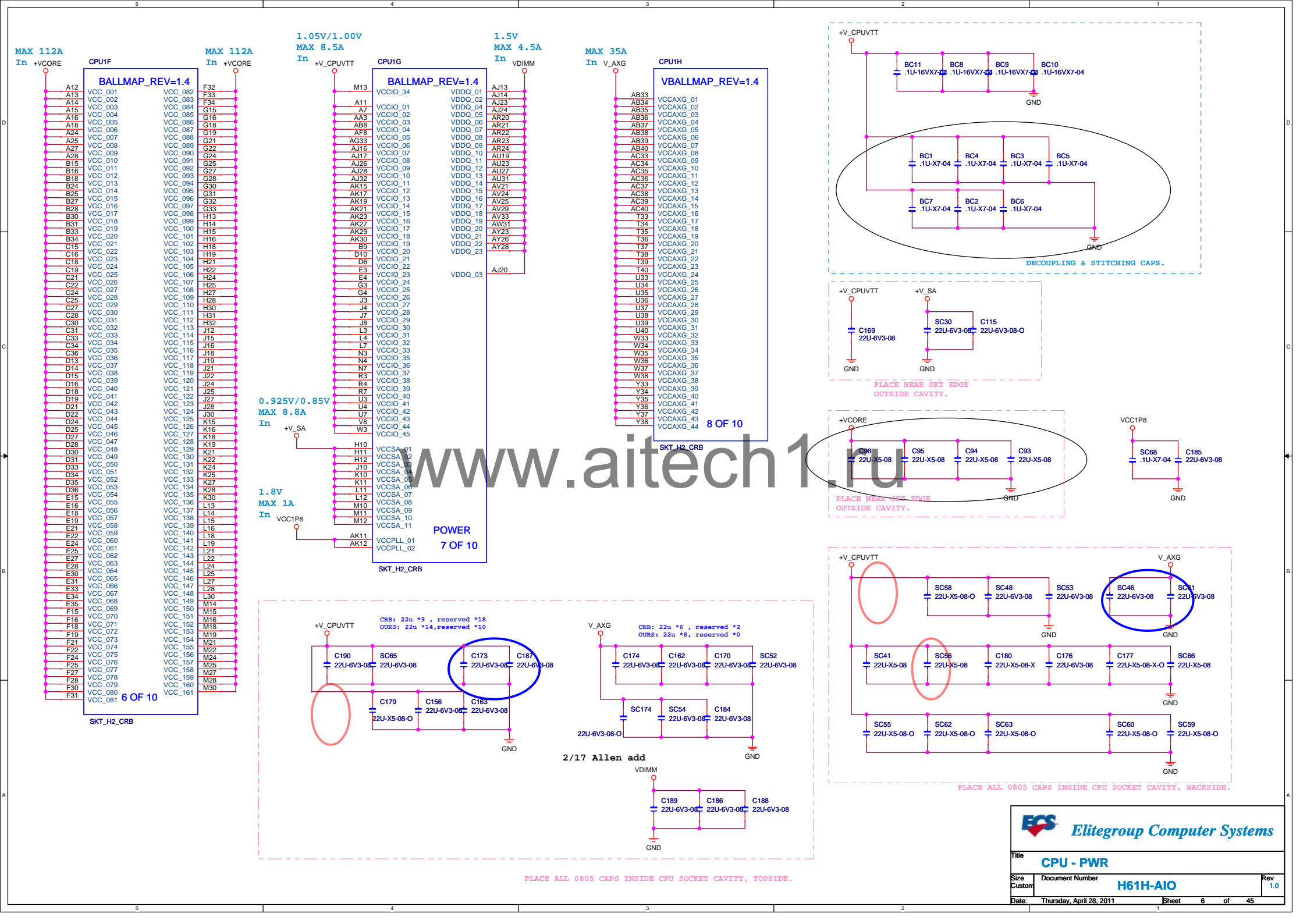


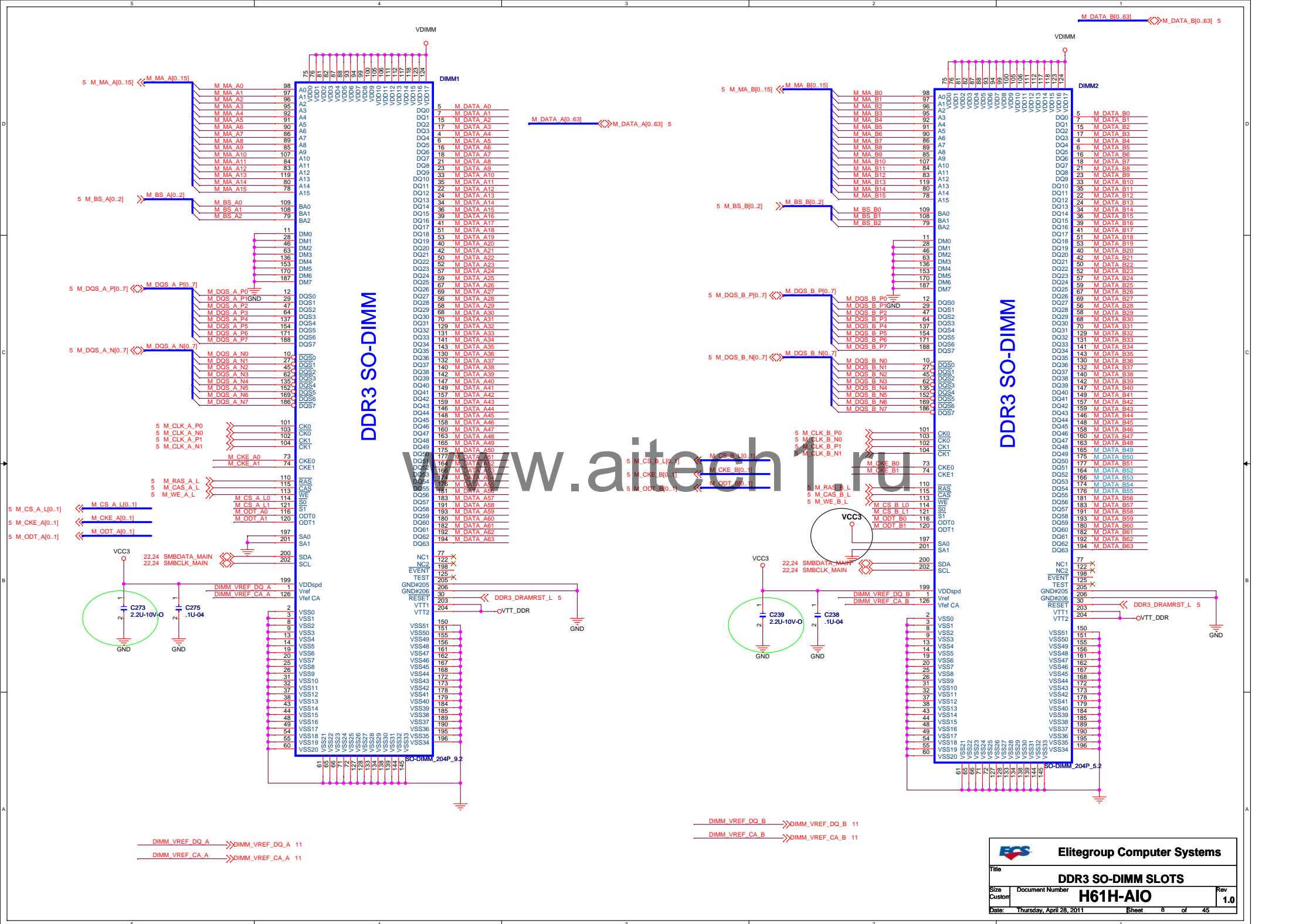
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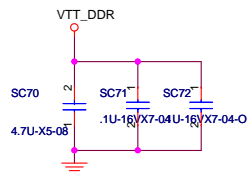
Pay Attention to This Part!



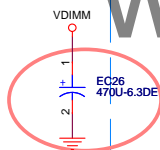
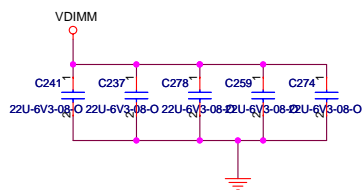
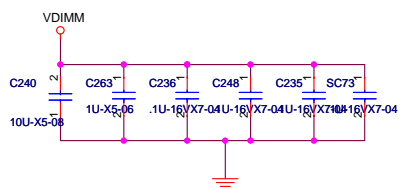
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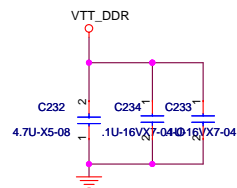




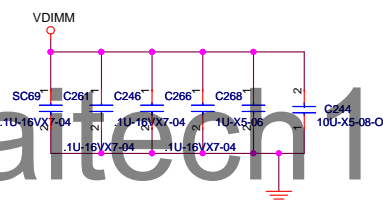
Layout: Close to DIMM0



3/3 allen ch bom

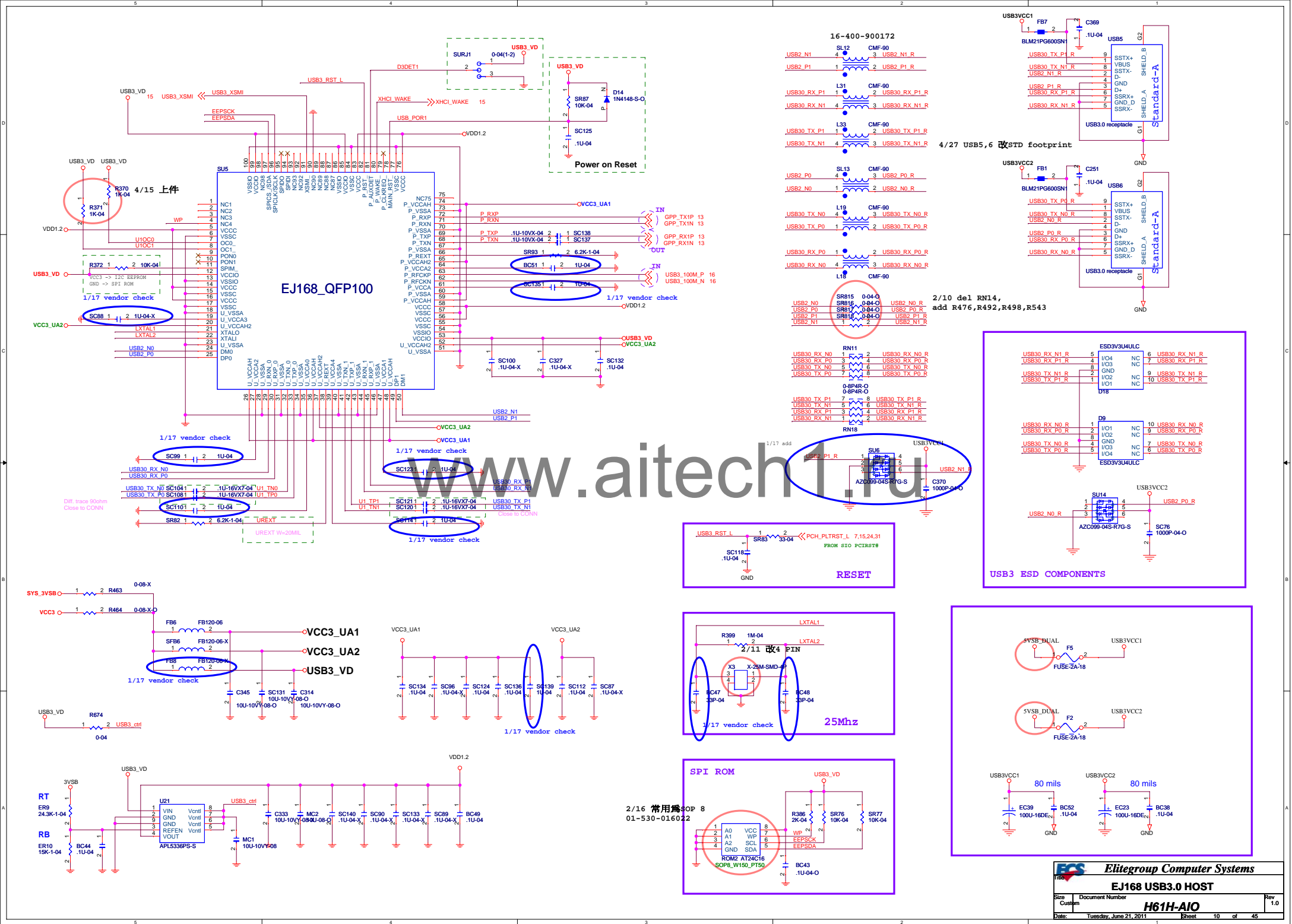


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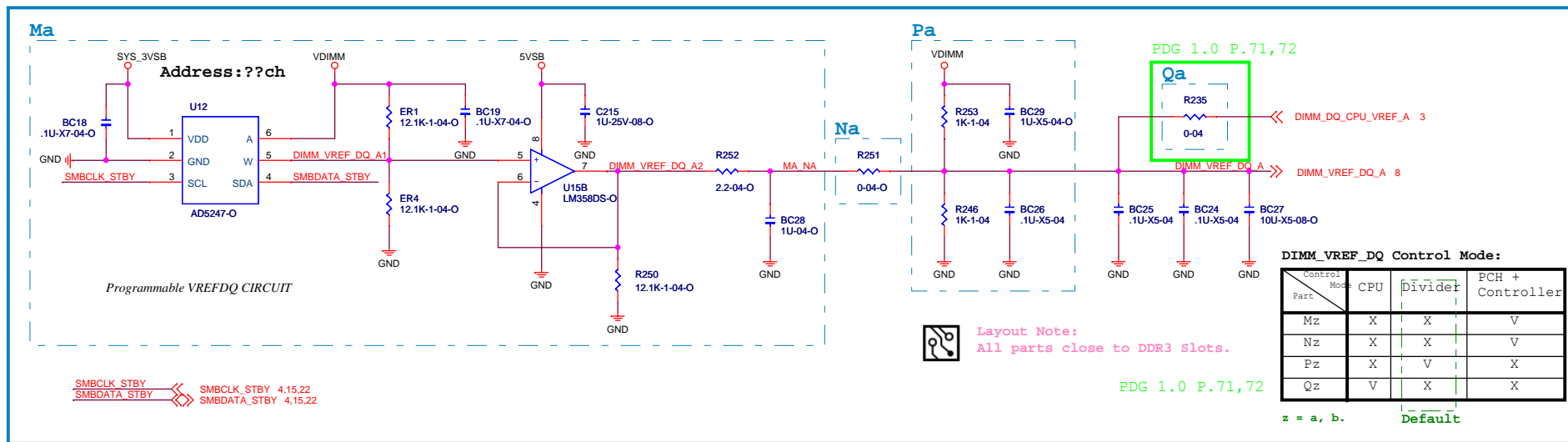


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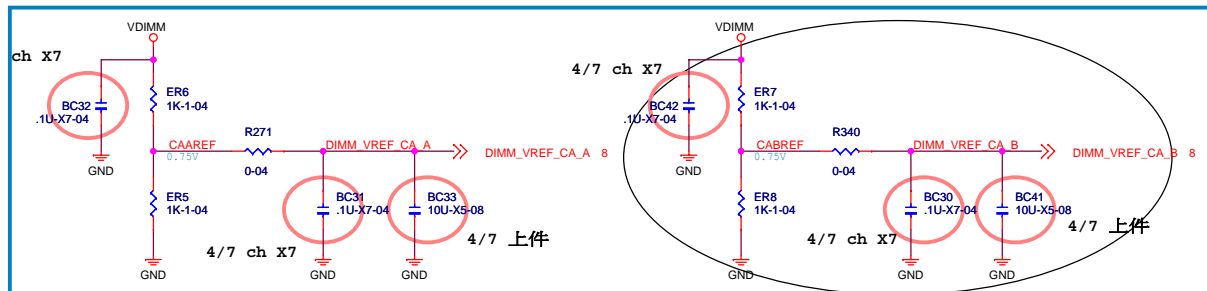
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Size			H61H-AIO
Document Number			Rev 1.0
Date: Tuesday, May 17, 2011			Sheet 9 of 45



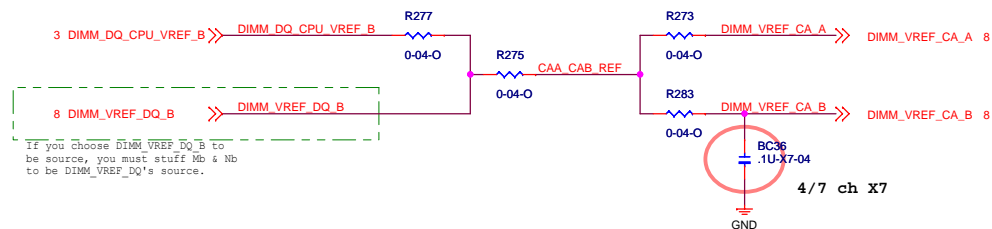
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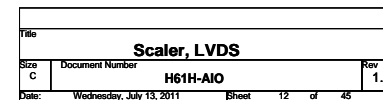


DIMM_VREF_DQ Control Circuit

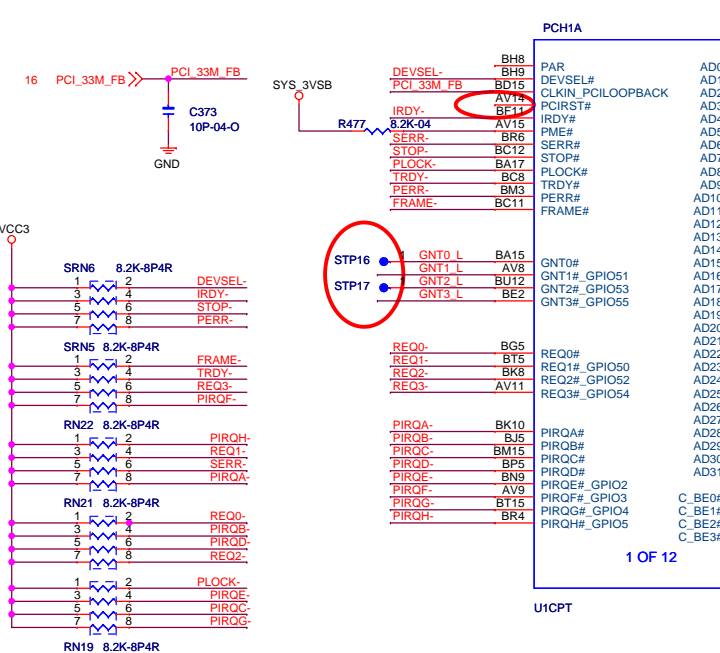


DIMM_VREF_CA Circuit





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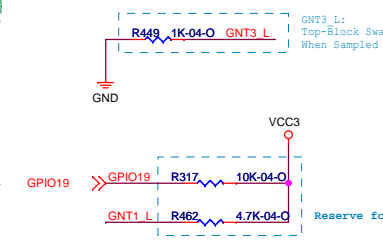


Boot Device Select:

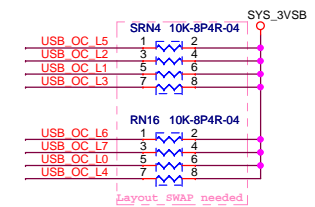
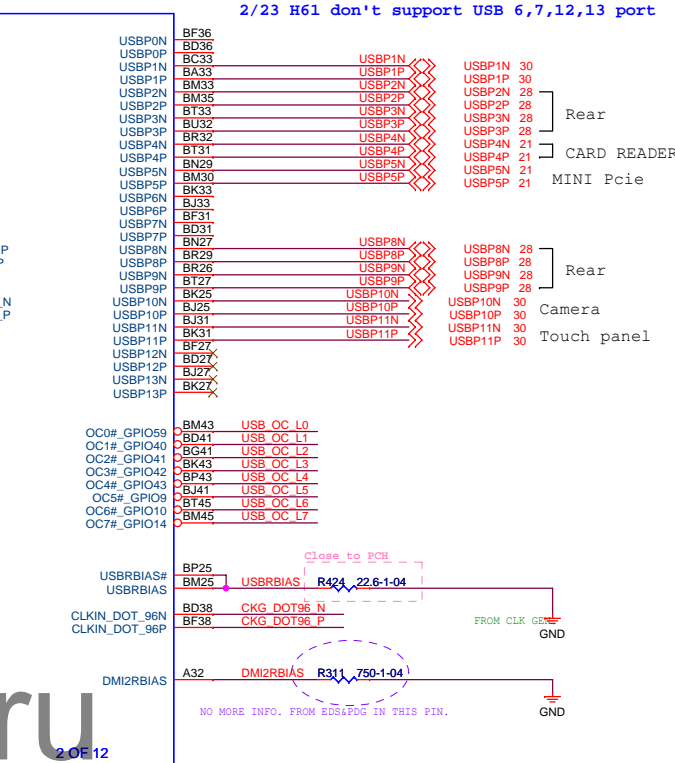
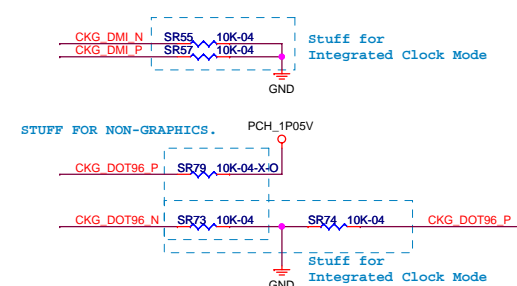
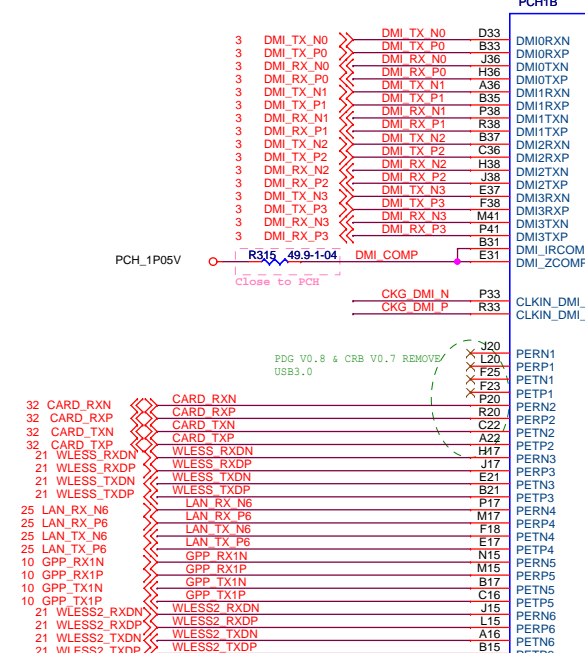
BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

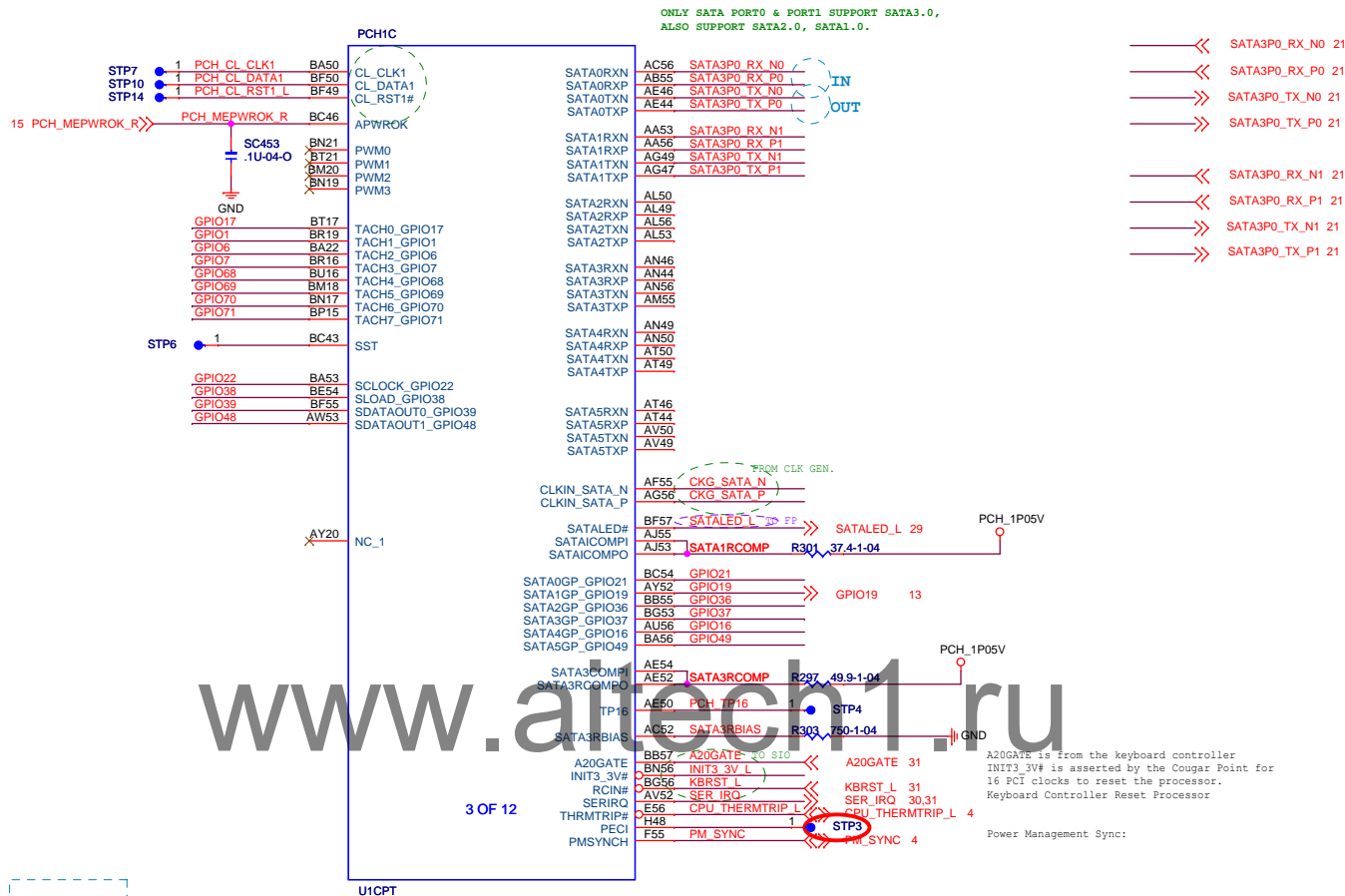
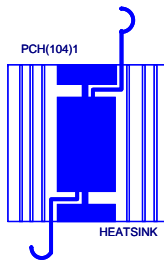
* GNT1[0..3]# GPIO19 have been internal pull high to +VCC3

GNT1#, GPIO19 Follow CPT EDS V0.7, CRB V0.7, PDG V0.8



GNT3_L: Top-Block Swap Override Mode, When Sampled Low.

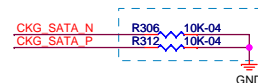
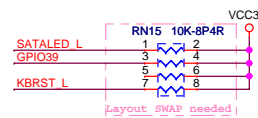
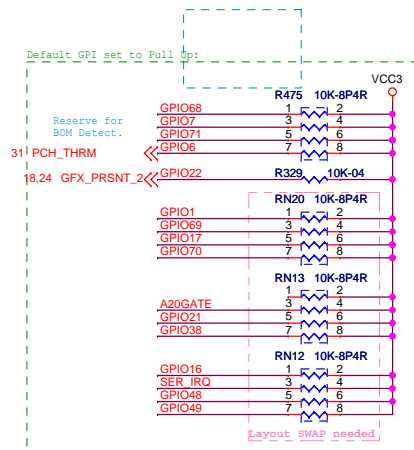




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GPIO36_TCM_PST_L, GPIO37_TCM:
TCM Header in Enable TCM,
Disable TPM.

GPIO16, GPIO49:
Reserve for TPM.



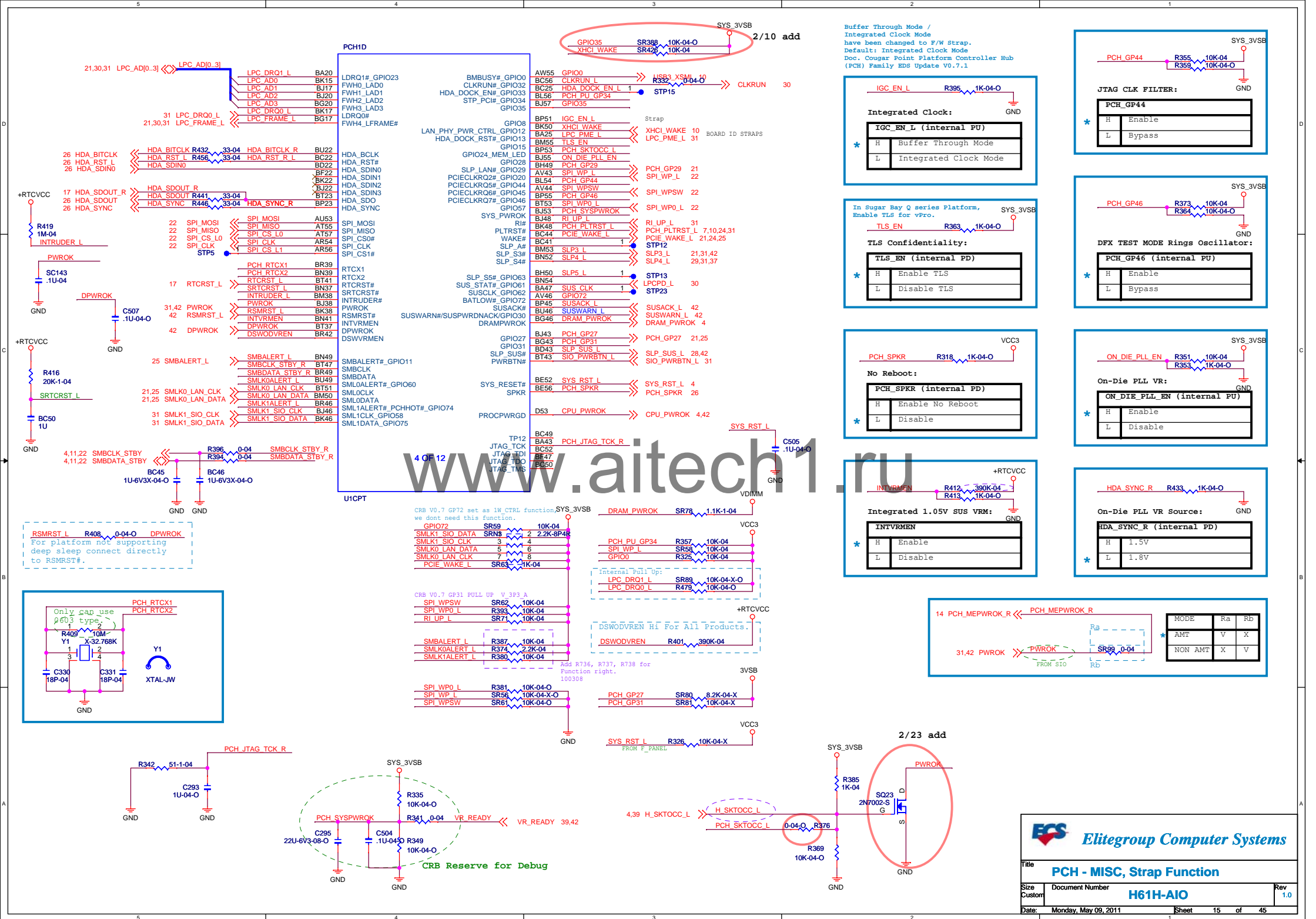
Stuff for Integrated Clock Mode

2/1 ch pull down to pull high

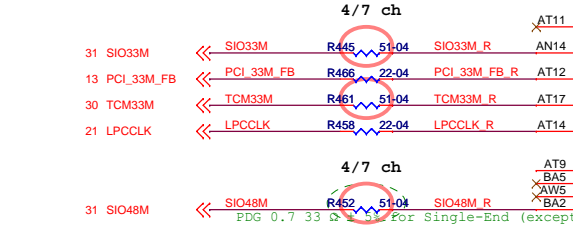
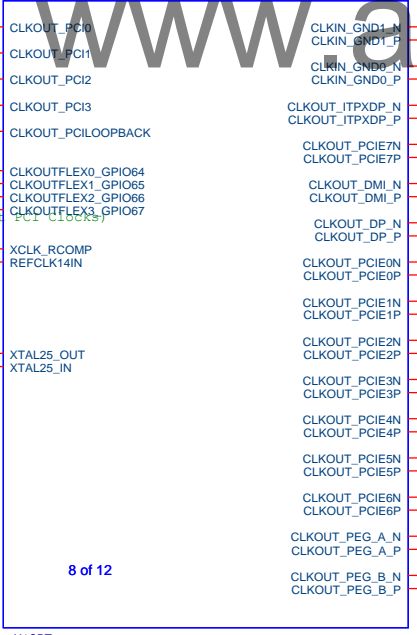


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Title		PCH - SATA, SATA CONN
Size	Document Number	H61H-AIO
Custom		Rev 1.0
Date:	Monday, May 09, 2011	Sheet 14 of 45

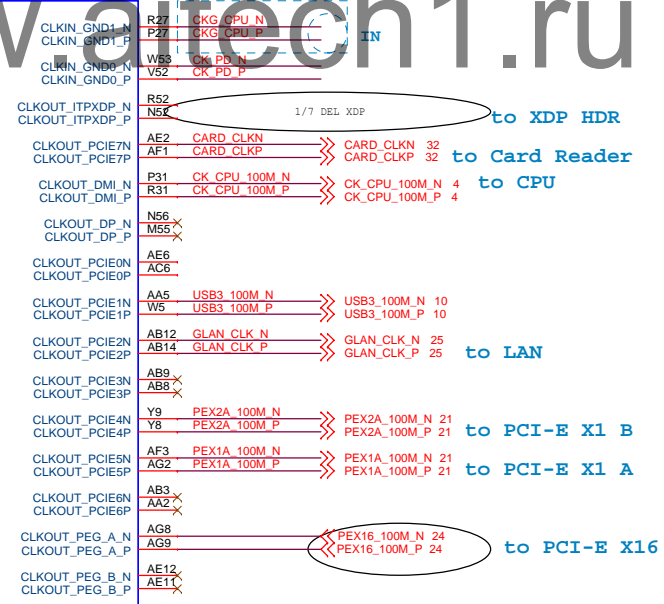
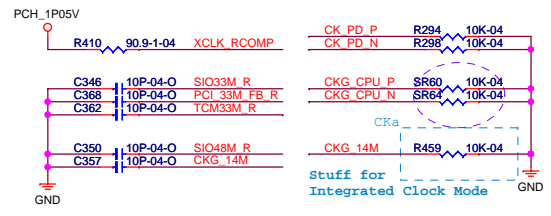
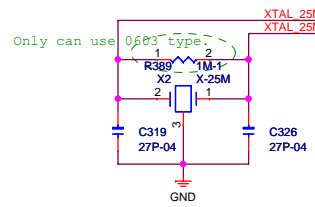


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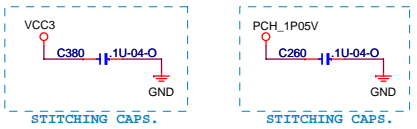


External pull-down input termination is required in Integrated Clock Generation mode and when no external clock chip is present

Layout Note:
PCI Clock Max 15000MILS



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Clock Mode	CLK GEN. IDT CV184 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X

Title
PCH - CLK IO

Size
Custom

Document Number
H61H-AIO

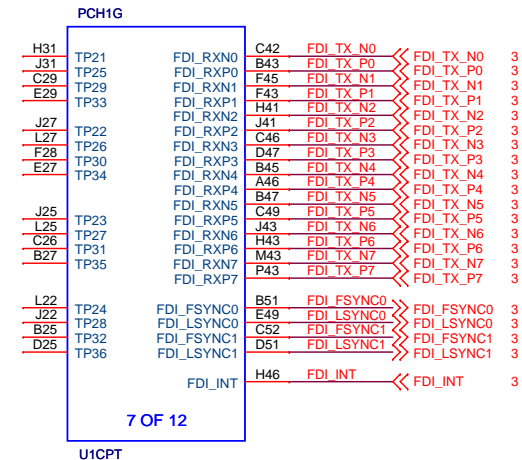
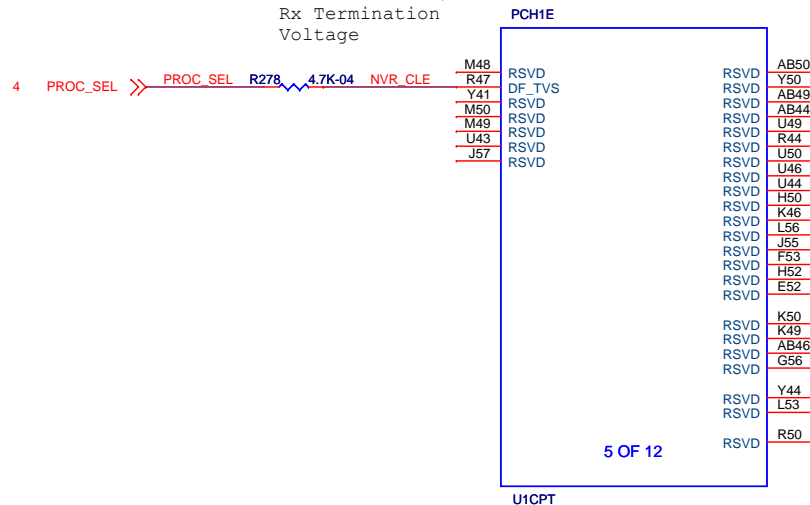
Rev
1.0

Date: Thursday, April 28, 2011

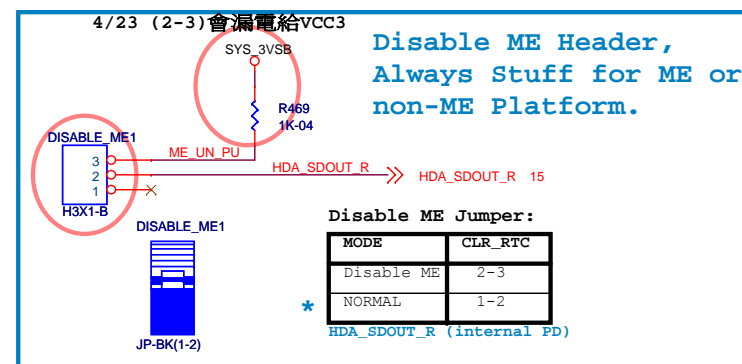
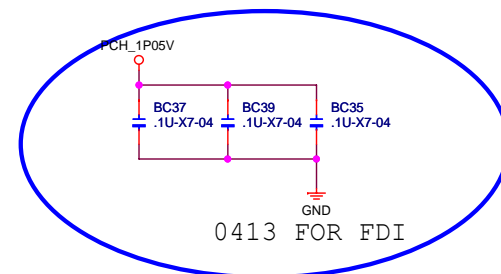
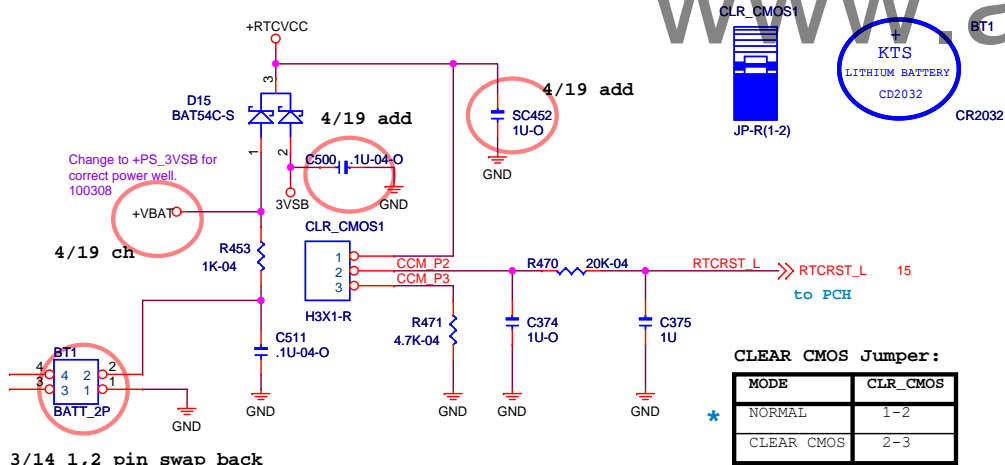
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This pin should be pulled up to 1.8 V or 3.3 V.

DMI and FDI Tx/
Rx Termination
Voltage



CLR_CMOS



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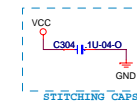
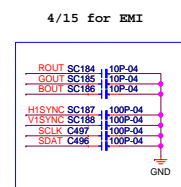
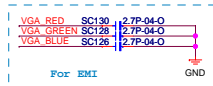
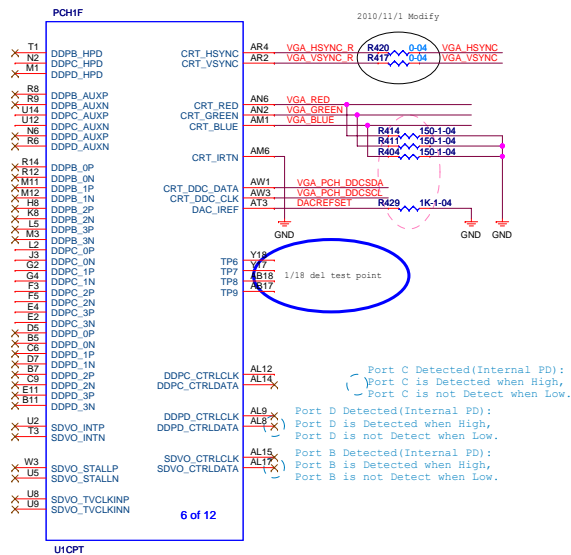
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Size Custom Document Number H61H-AIO

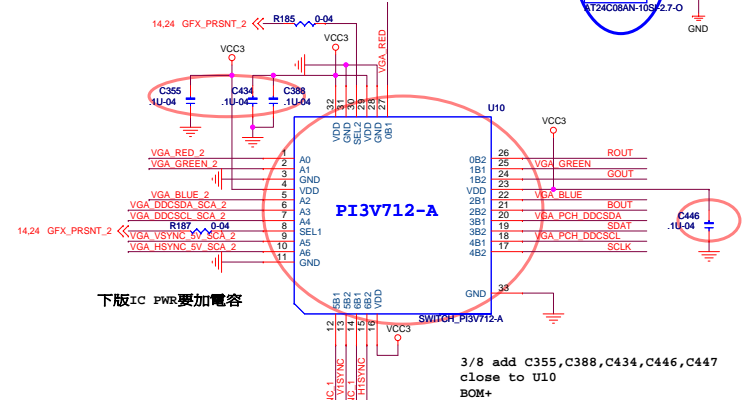
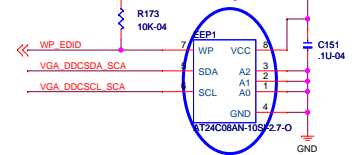
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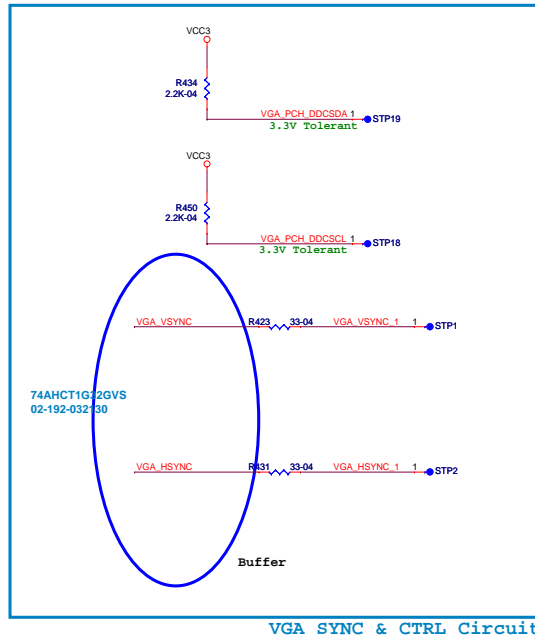
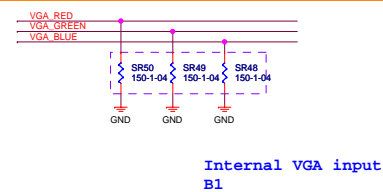
Rev 1.0



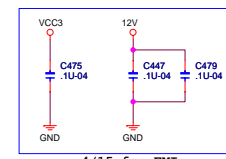
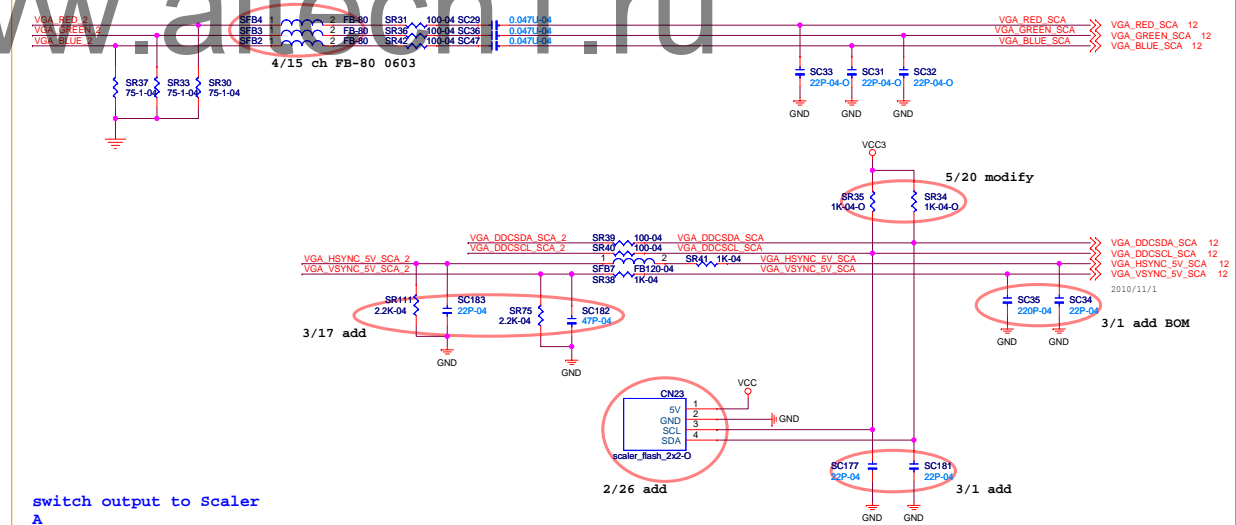
2/10 ch -O
上線前發工單

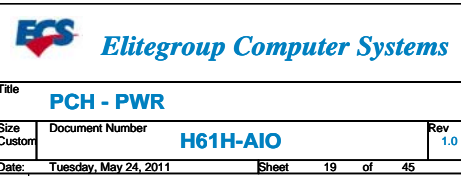


下版IC PWR要加電容

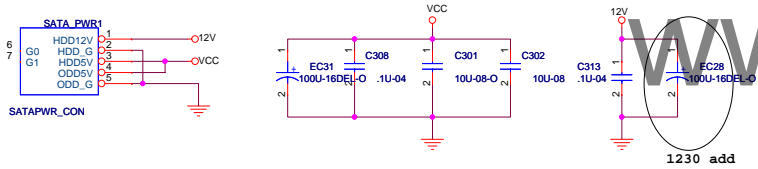
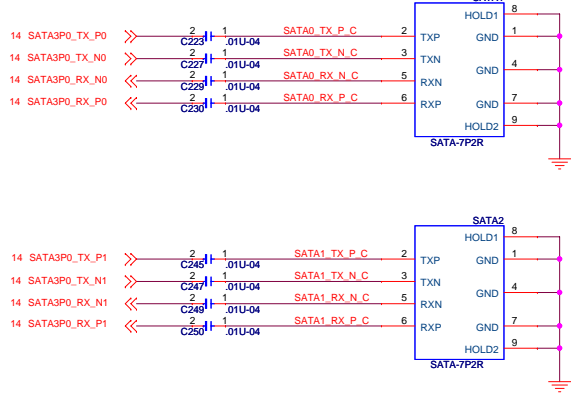


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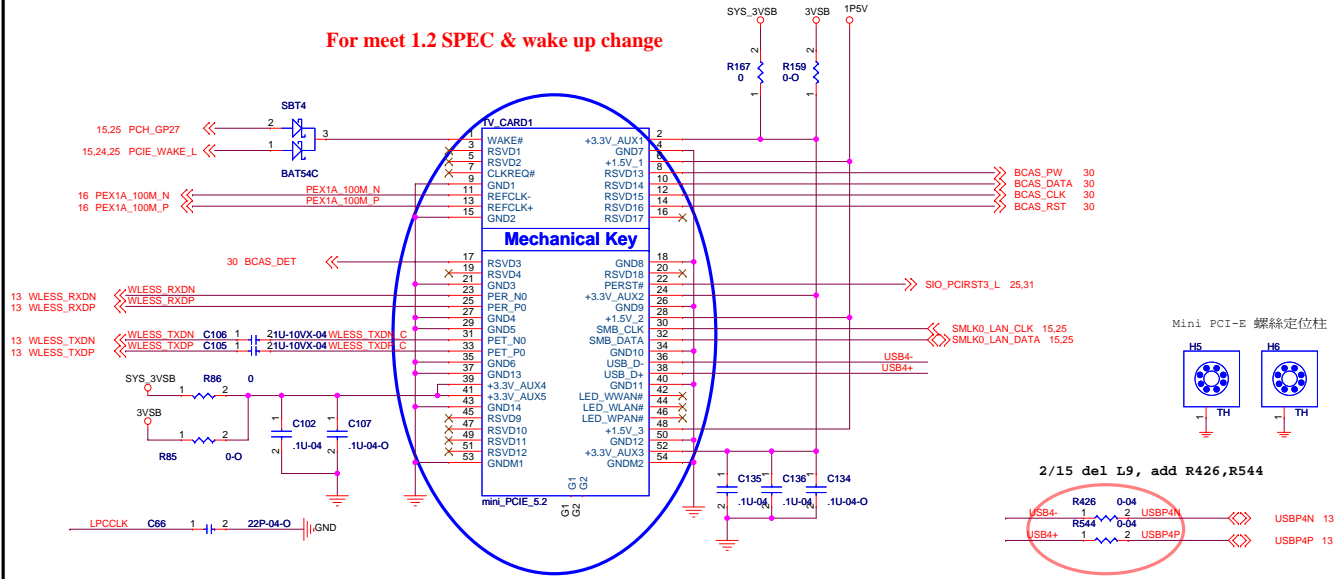


SATA



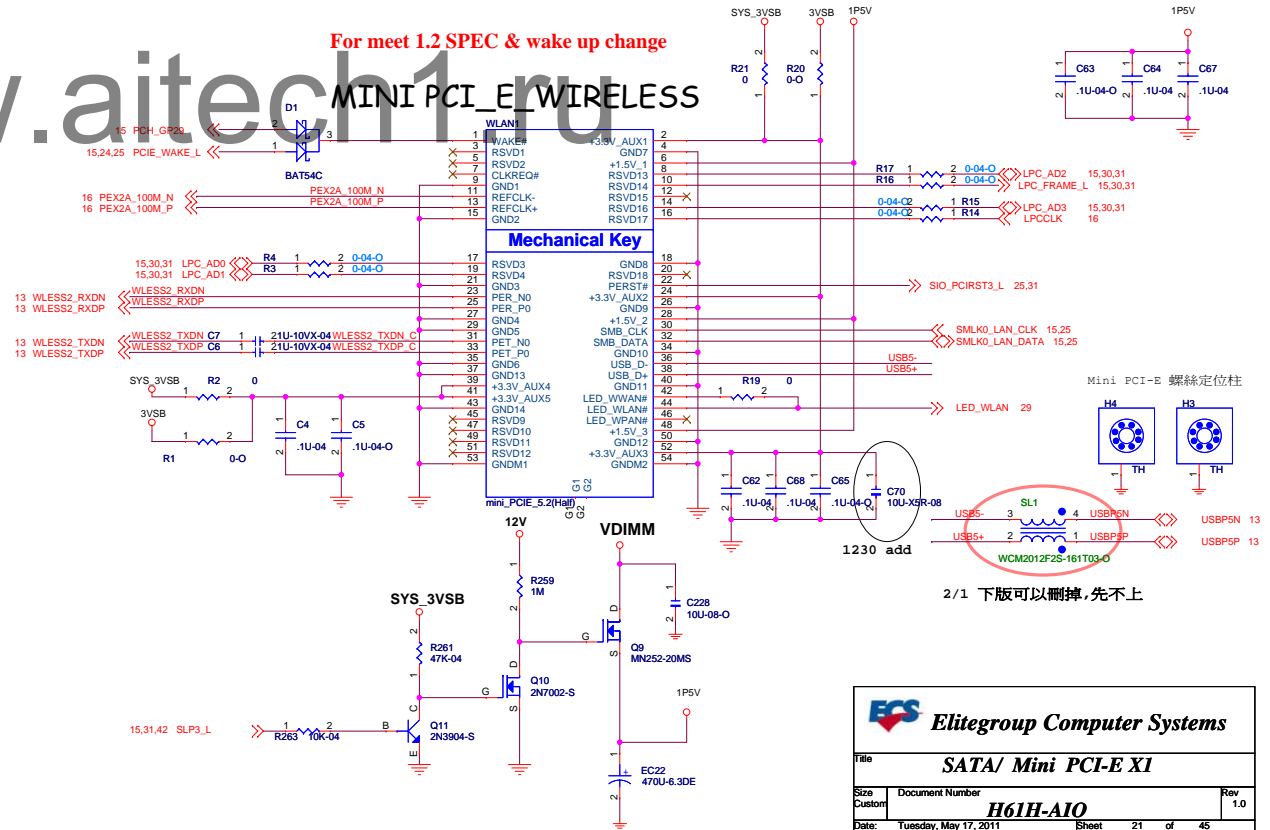
1230 add

For meet 1.2 SPEC & wake up change

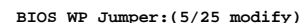


For meet 1.2 SPEC & wake up change

MINI PCI_E_WIRELESS



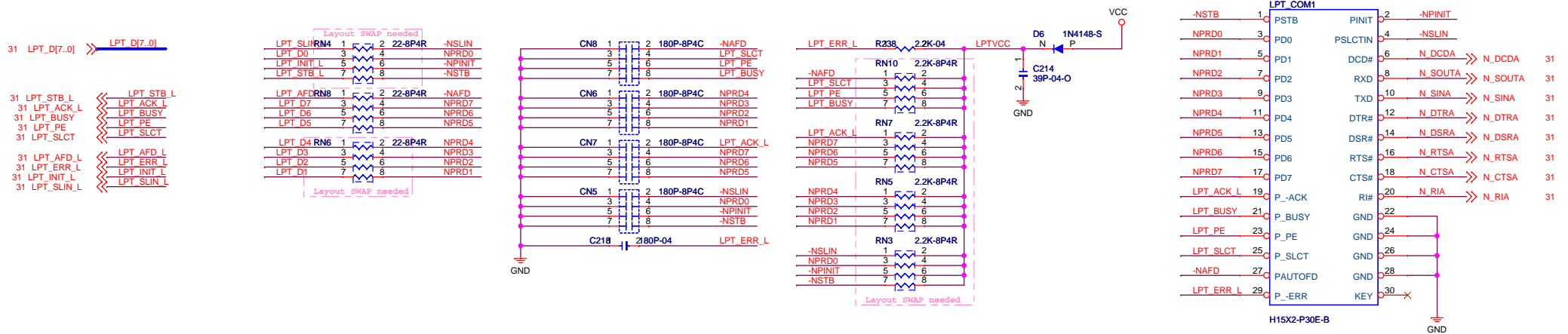
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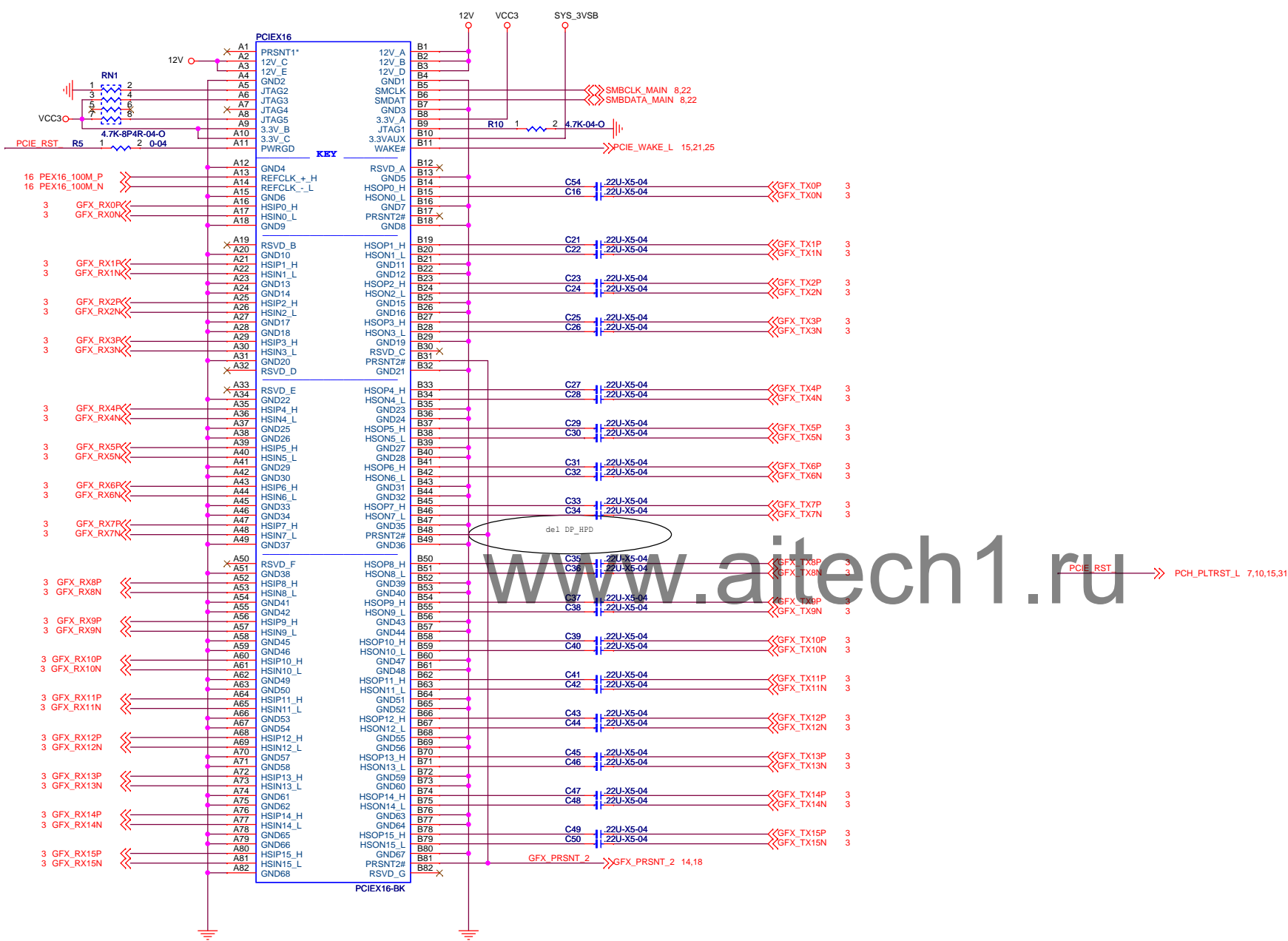
BIOS_WP	
1-2	BIOS_WP
2-3	NORMAL



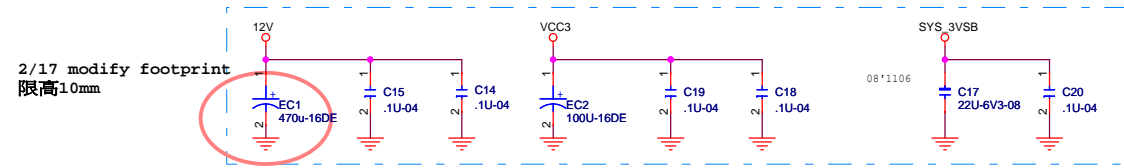
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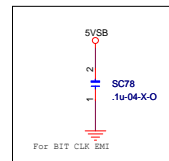
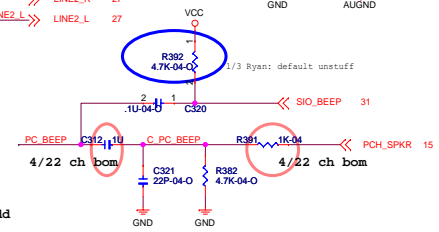
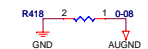
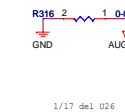
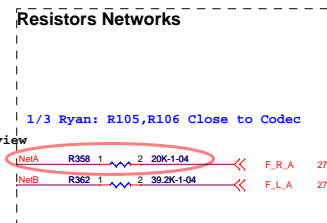
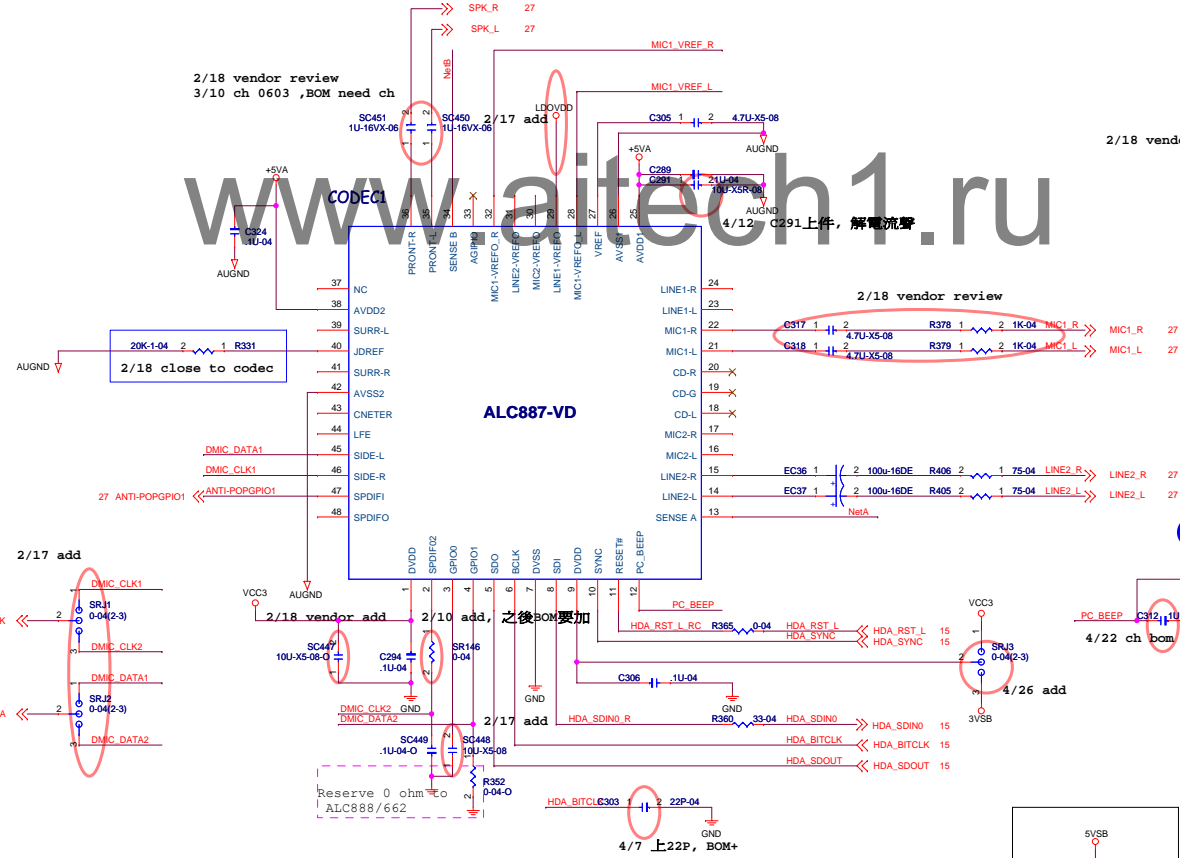
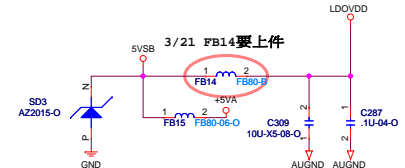
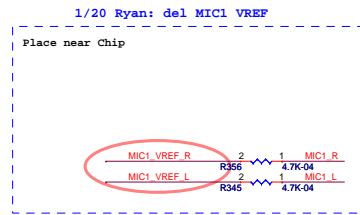
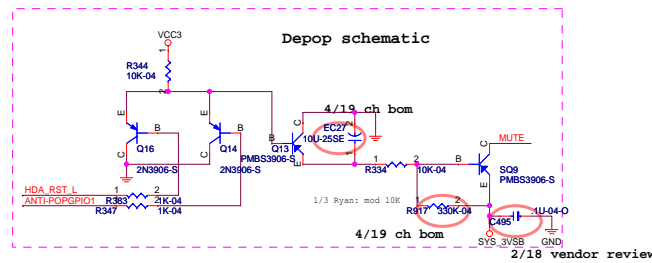
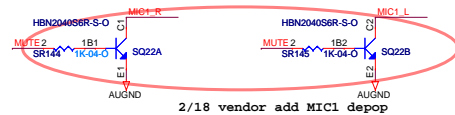


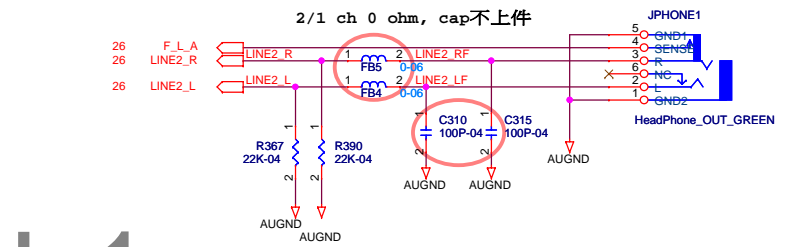
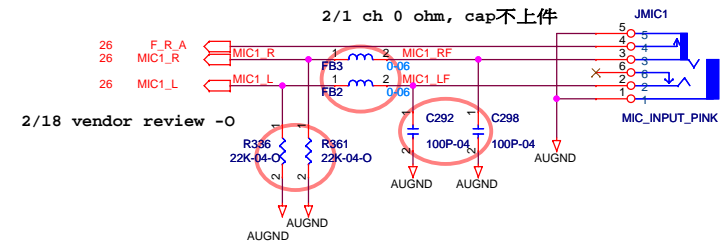
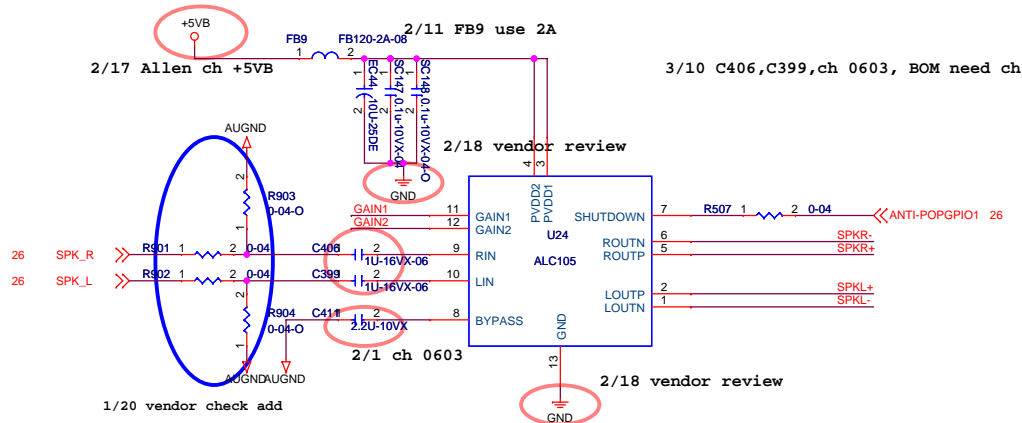
LPT&COM Header Circuit



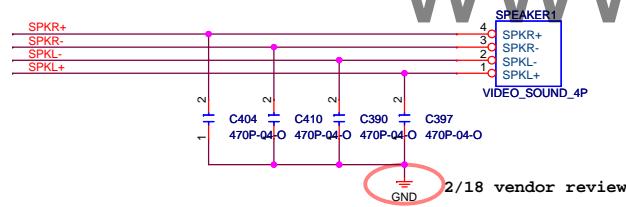
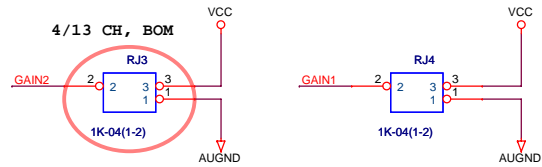
Please place the caps close to PCIe16 Slot.







GAIN1	GAIN2	Single-End	Differential
(Default) 0	0	5dB	11dB
1	0	8dB	14dB
0	1	13dB	19dB
1	1	19dB	25dB

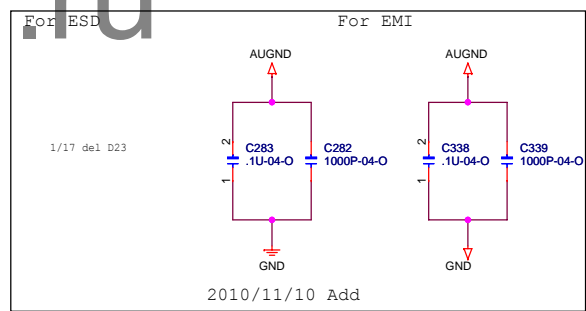
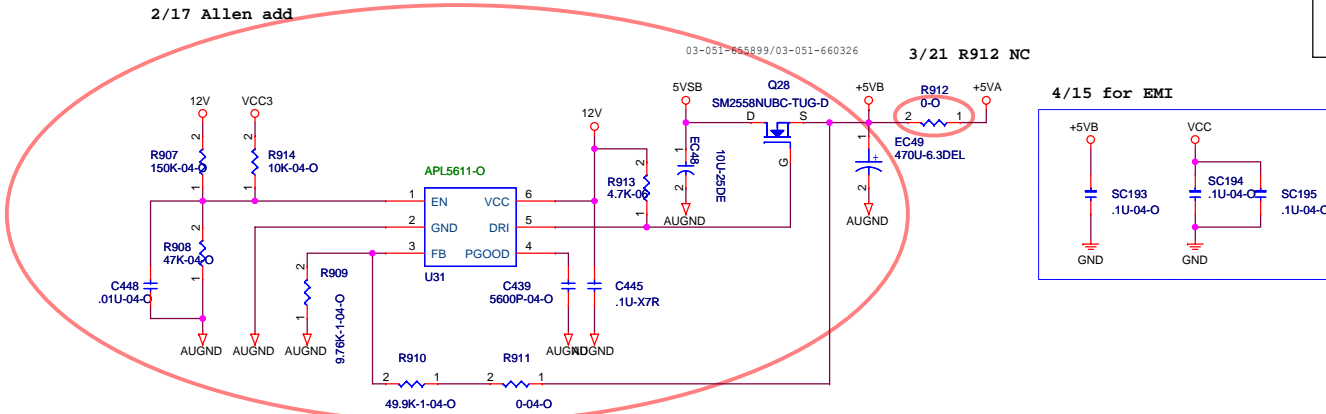


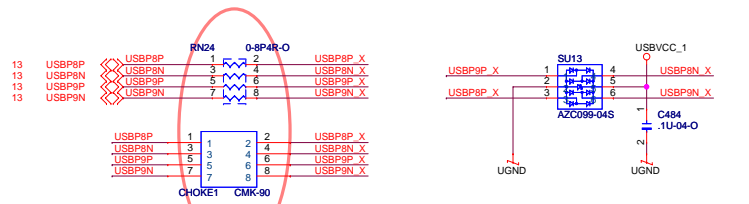
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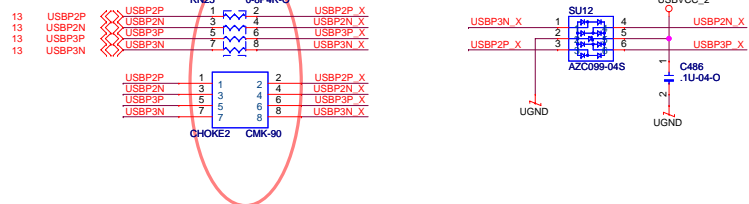
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4/15 for EMI

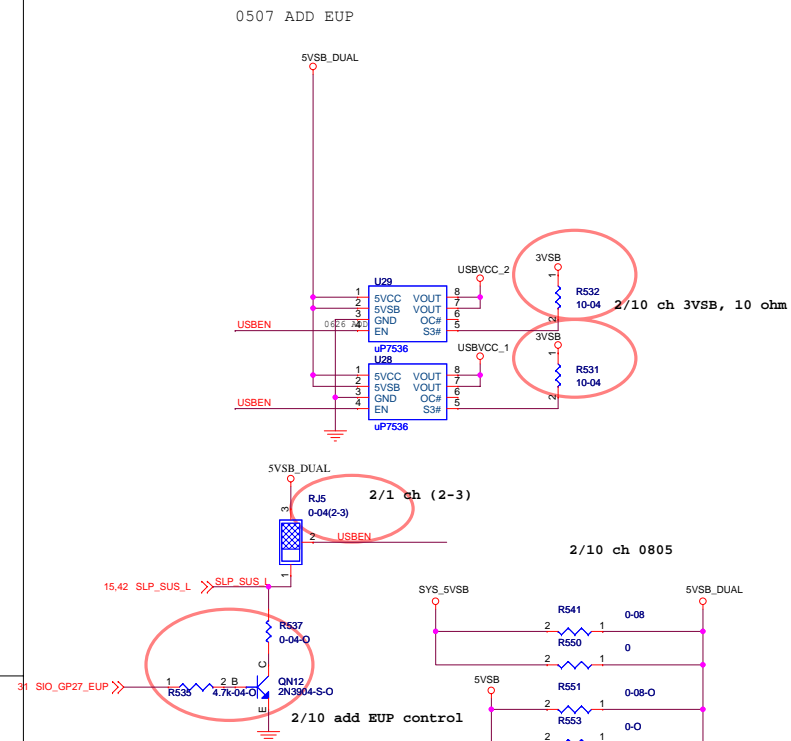
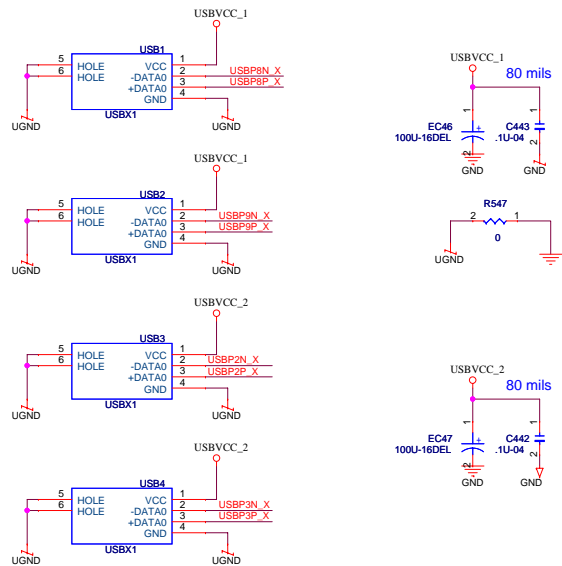




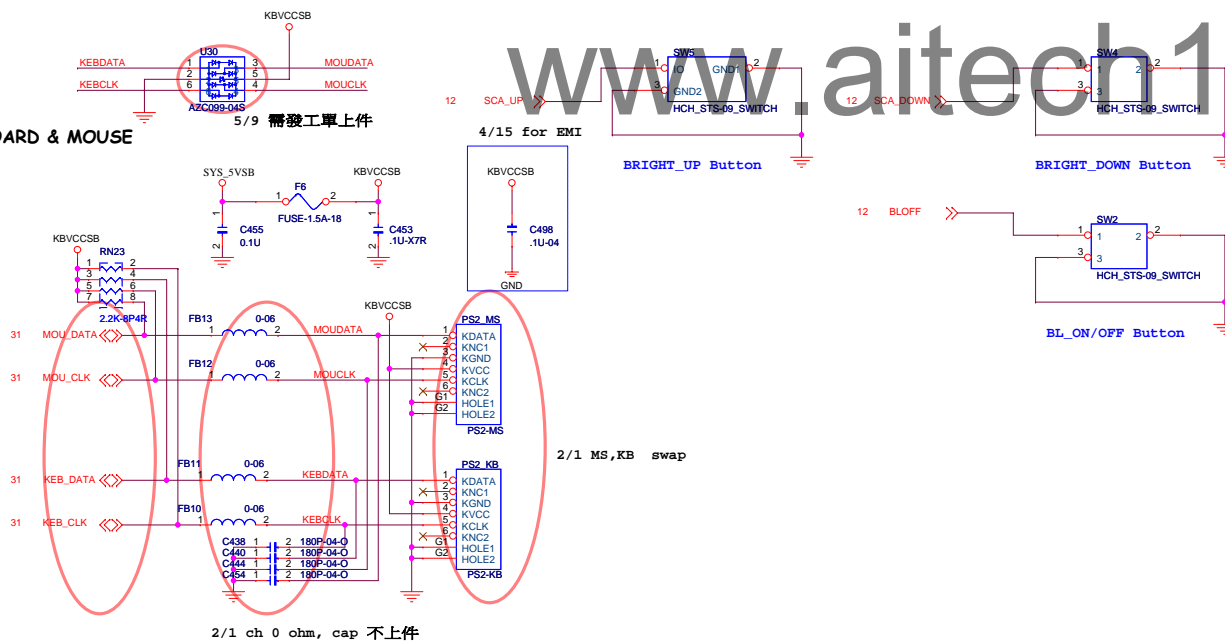
2/1 ch 0 ohm



Rear Panel



KEYBOARD & MOUSE

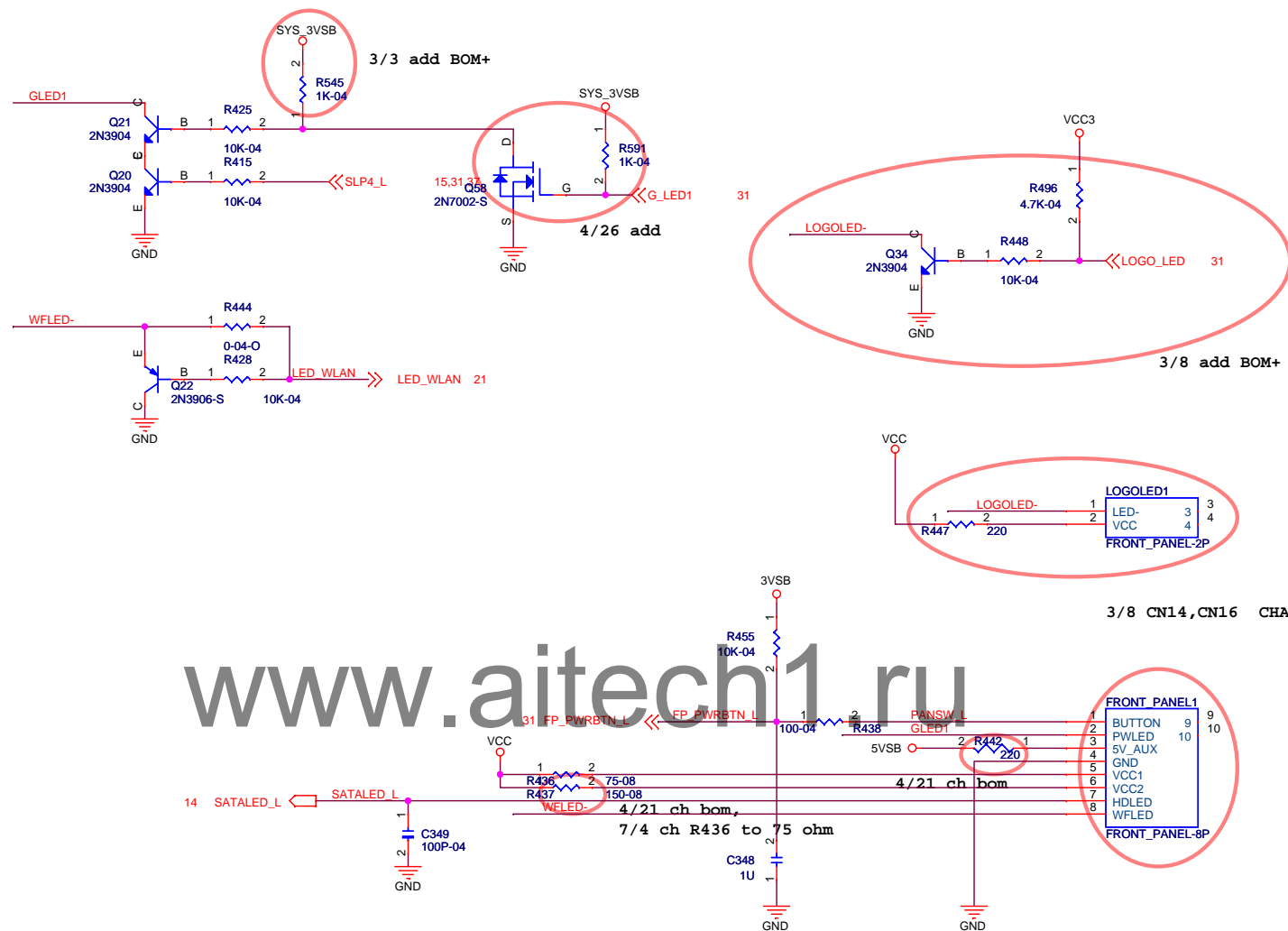


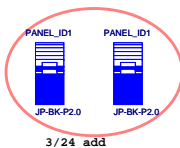
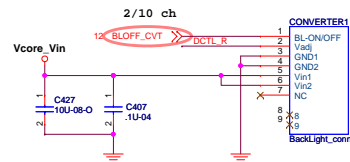
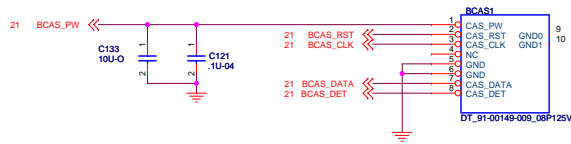
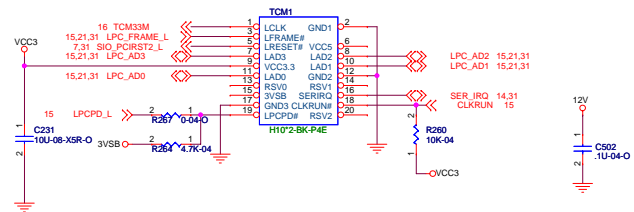
2/1 ch 0 ohm, cap 不上件

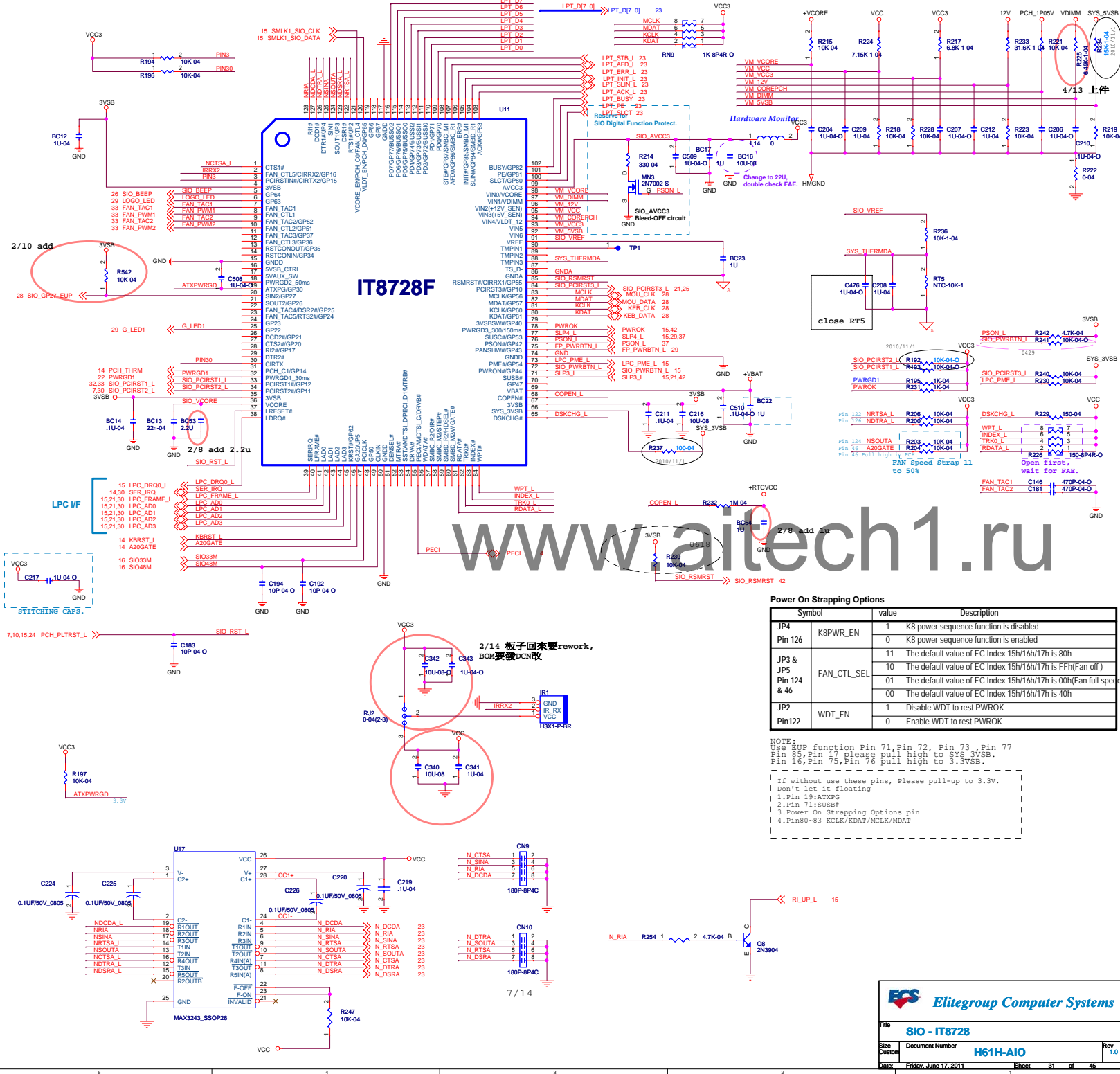
2/1 MS,KB swap

Front Panel

Elitegroup Computer Systems			
USB Port			
File	USB Port		
Size	Document Number	H61H-A10	
Custom			Rev 1.0
Date:	Tuesday, June 21, 2011	Sheet	28 of 45





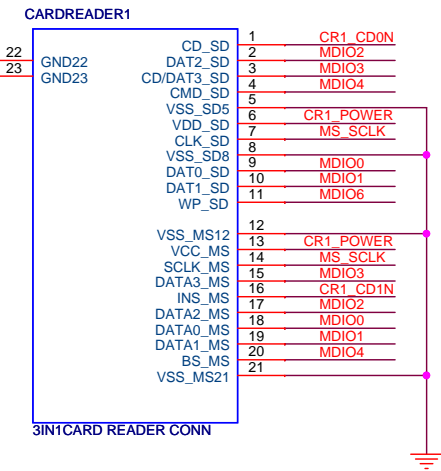
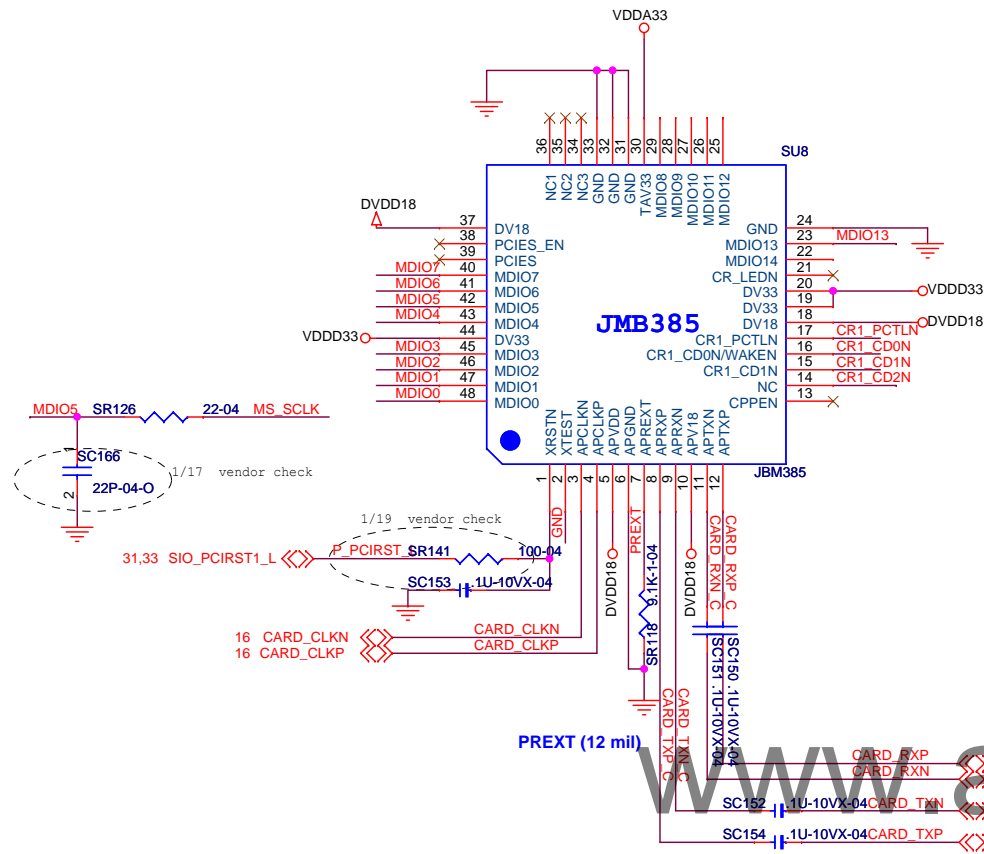


Power On Strapping Options

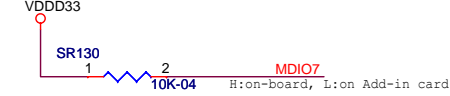
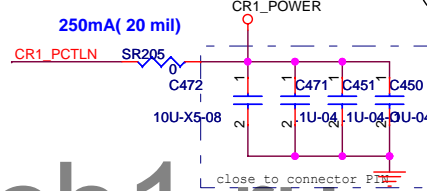
Symbol	value	Description
JP4	1	K8 power sequence function is disabled
Pin 126	0	K8 power sequence function is enabled
JP3 & JP5	11	The default value of EC Index 15h/16h/17h is 80h
Pin 124 & 46	10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
	00	The default value of EC Index 15h/16h/17h is 40h
JP2	1	Disable WDT to rest PWROK
Pin122	0	Enable WDT to rest PWROK

NOTE:
Use SUP function Pin 71, Pin 72, Pin 73, Pin 77
Pin 85, Pin 17 please pull high to SYS 3VSB.
Pin 16, Pin 75, Pin 76 pull high to 3.3VSB.

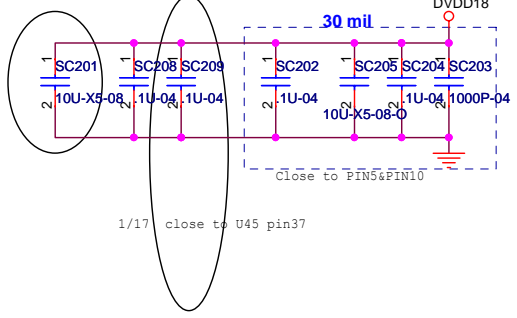
If without use these pins, Please pull-up to 3.3V.
Don't let it floating
1. Pin 19: ATXPG
2. Pin 71: SUSBP#
3. Power On Strapping Options pin
4. Pin80-83 KCLK/KDAT/MCLK/MDAT



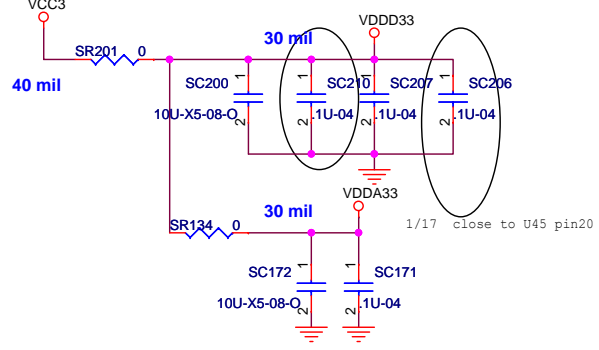
1/17 vendor check del
SBT2, SC115



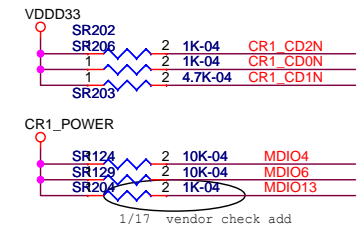
1/17 vendor check close to U45 pin18



1/17 close to U45 pin44



1/17 vendor check del
Reserve circuit for debugging



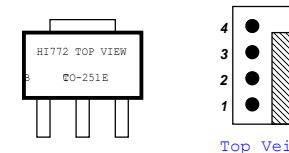
1/17 vendor check add

Elitegroup Computer Systems

Title **Card reader (JMB385)**

Size Custom Document Number **H61H-AIO** Rev B

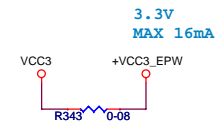
Date: Tuesday, May 17, 2011 Sheet 32 of 45



1/7 DEL

1/7 DEL


PCH_MEPWROK Circuit



VCC3_EPW control

VCC3 Net to +VCC3_EPW FOR
NON-INTEL LAN (NO WOL) OR M0 ONLY

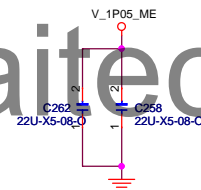
www.aitech1.ru

 <i>Elitegroup Computer Systems</i>		
Title DC/DC 3VDUAL		
Size Custom	Document Number H61H-AIO	Rev 1.0
Date: Thursday, April 28, 2011	Sheet 34	of 45

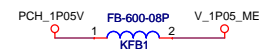
V_1P05_ME

08-463-225092
2.2uH DCR 60mOhm

1.05V@1.7A Max



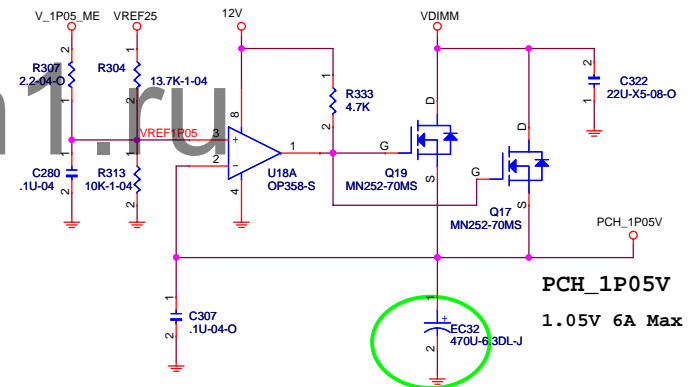
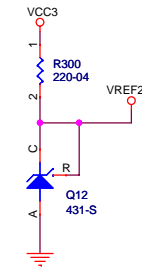
04-807-226692
22uF 6.3V X5R



For Non-AMT

EMPTY EVERYTHING ELSE ON PAGE FOR NON AMT
STUFF KFB2 FOR NON AMT SYSTEM

VREF25



PCH_1P05V

1.05V 6A Max

ECS
Elitegroup Computer Systems

Title **DC-DC PCH_1P05**

Size Custom Document Number **H61H-A10** Rev 1.0

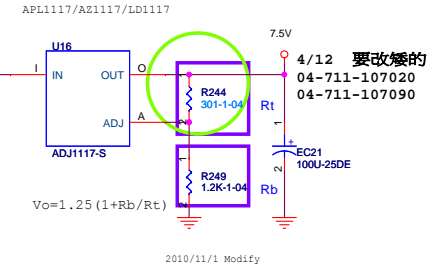
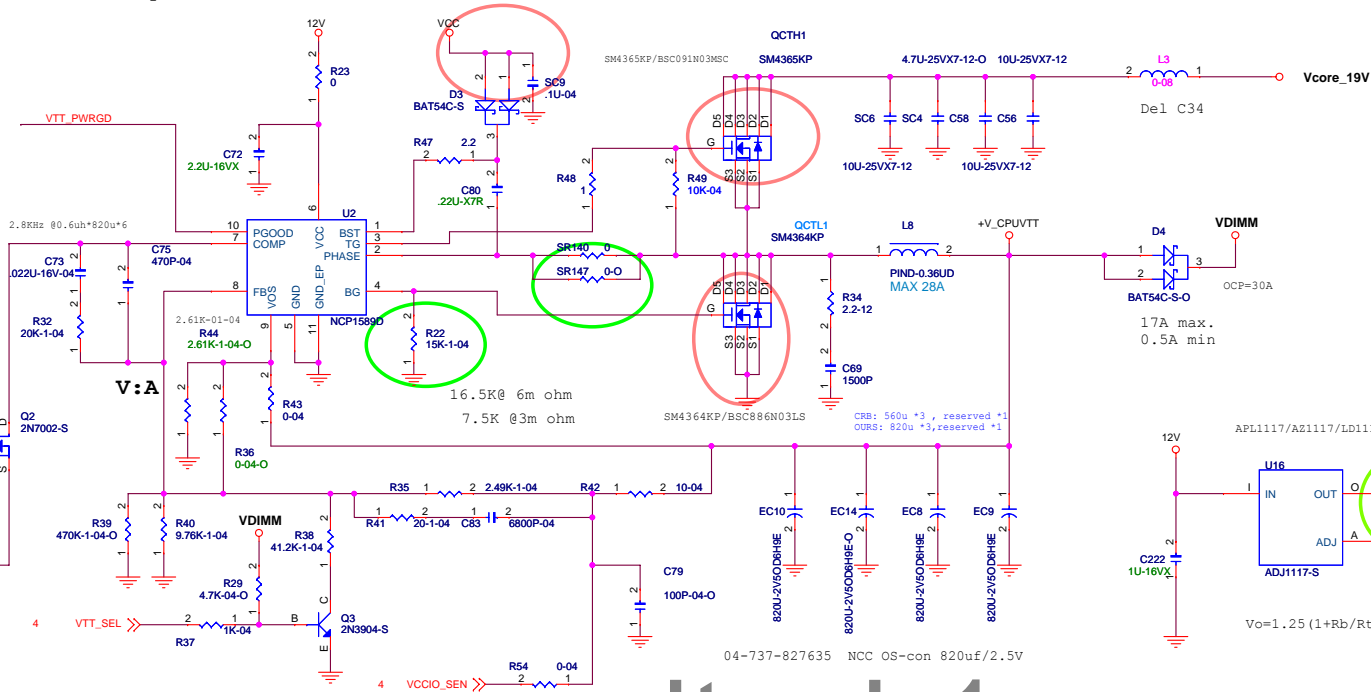
Date: Friday, June 17, 2011 Sheet 36 of 45

Delay:100ns~5ms

V_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

9.76K//41.2K=7.89K (7.87K)



Default Stuffed:

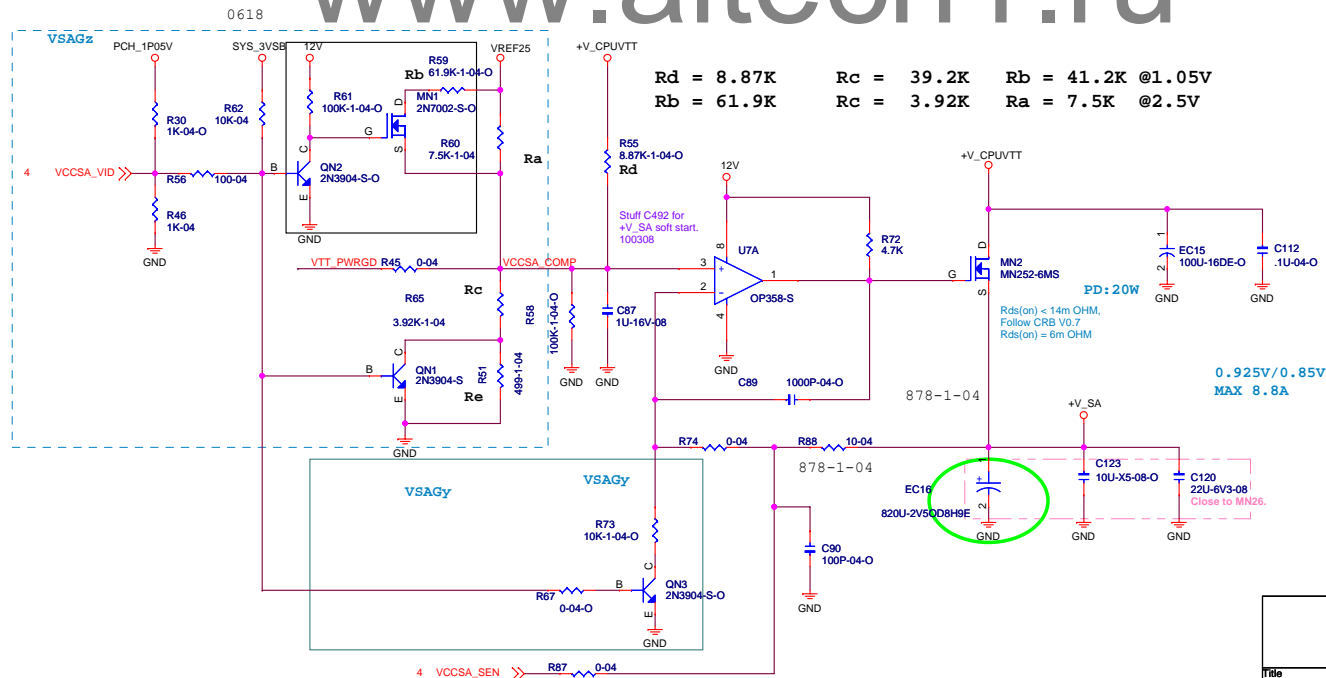
Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*

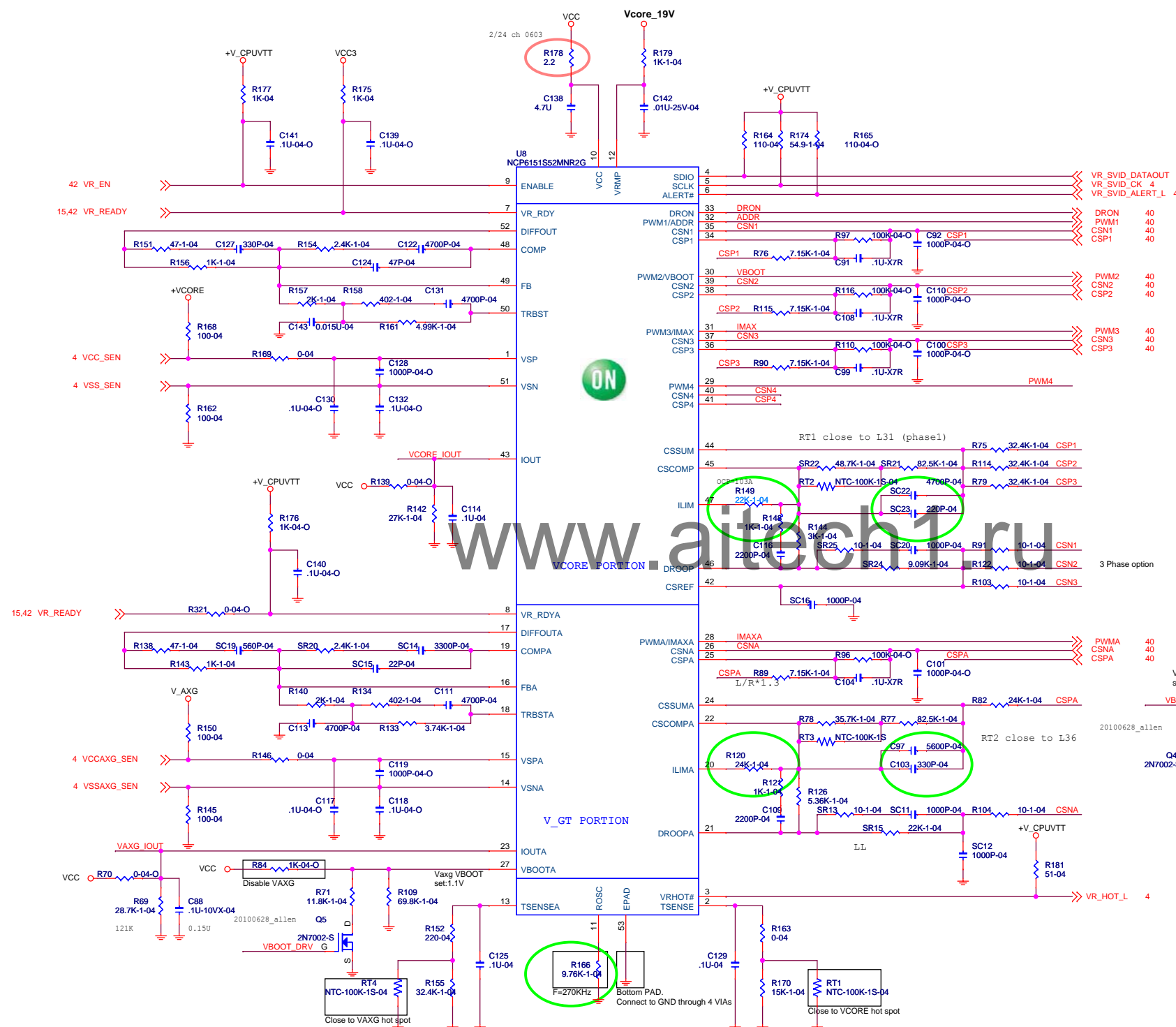
Stuff VSAGy

VCCSA voltage selection	
VID	+V_SA
0	0.85V
1	0.925V



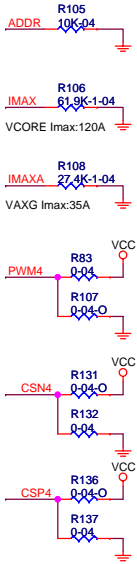
Elitegroup Computer Systems

Title		DC/DC V_CPUVTT
Size	Document Number	H61H-AIO
Custom		Rev 1.0
Date:	Tuesday, May 17, 2011	Sheet 36 of 45



PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR VAXG RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.90V
45K	1.0V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V

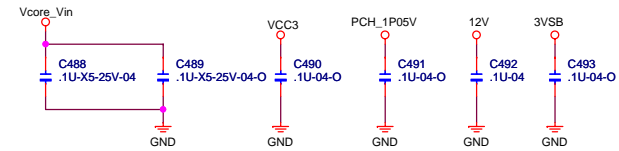


Title: **DC-DC:VCORE/VAXG1**

Size Custom: Document Number **H61H-AIO** Rev 1.0

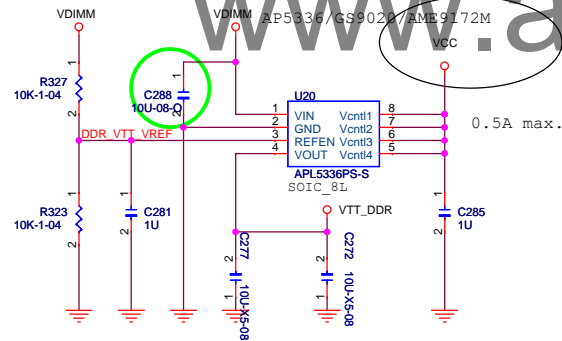
Date: Tuesday, May 17, 2011 Sheet 39 of 45

1/7 DEL XDP

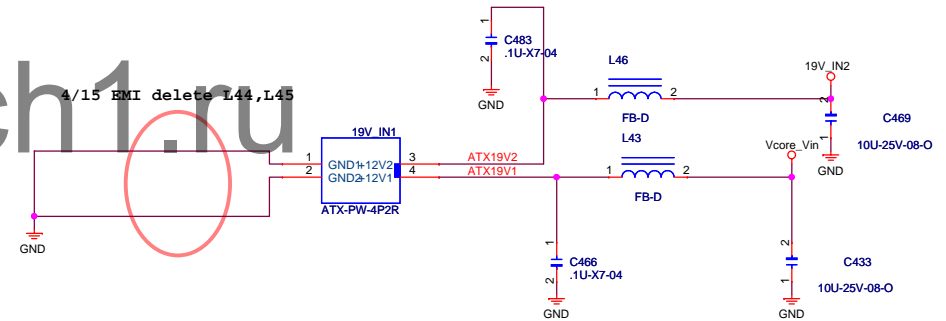


2/24 EMI add caps

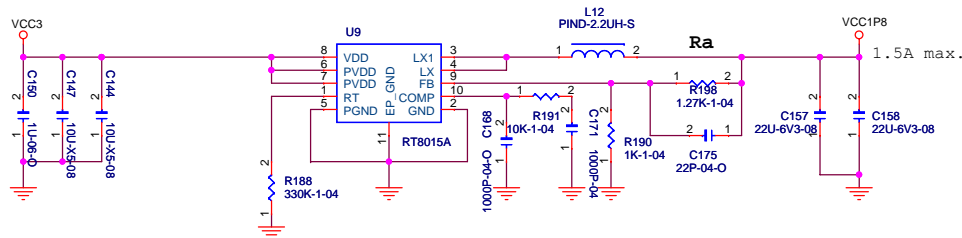
DDR VTT~0.83A (DDR3)



4/15 EMI delete L44,L45



08-463-225092
2.2uH DCR 60mOhm



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

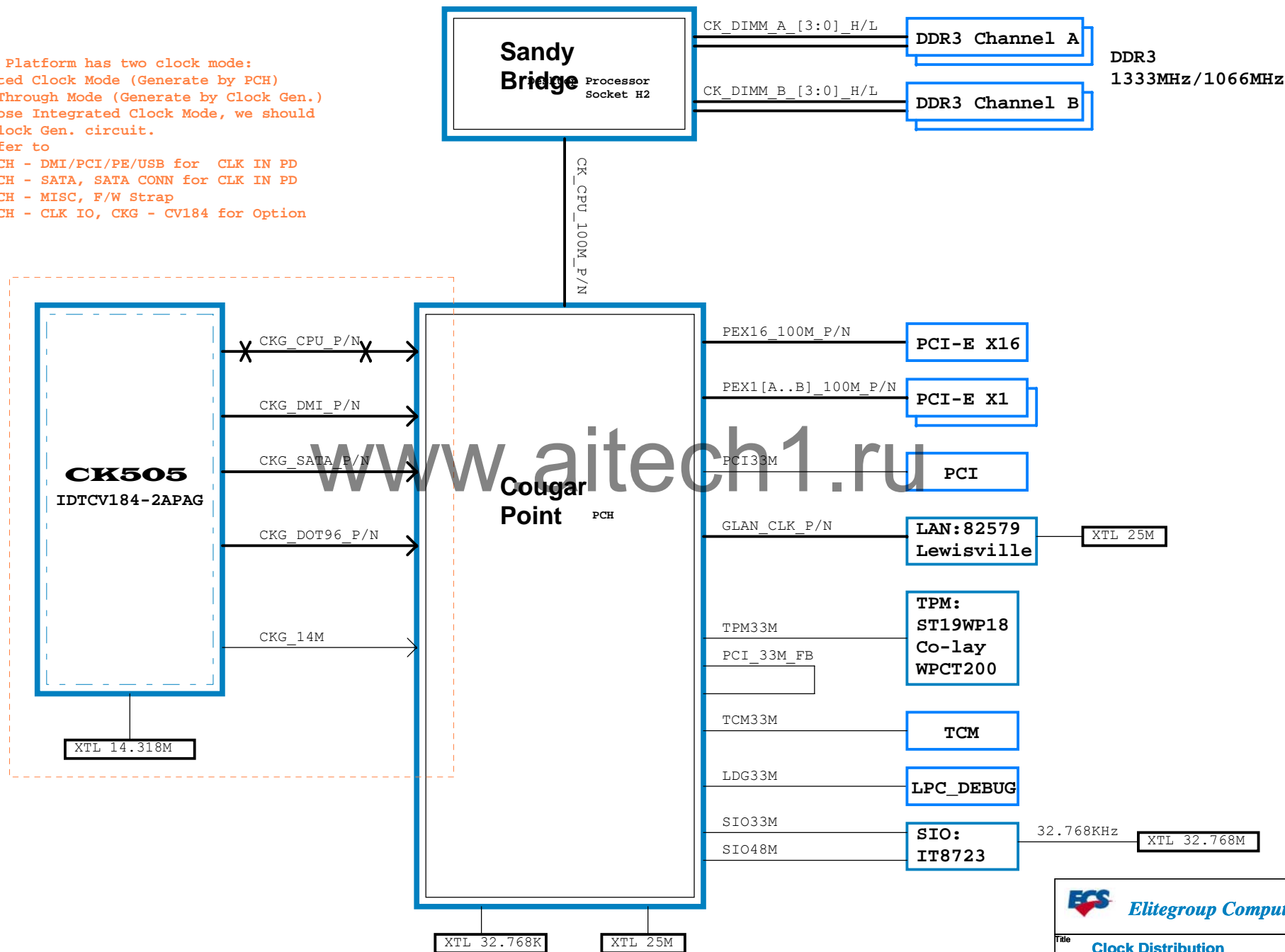
Please refer to

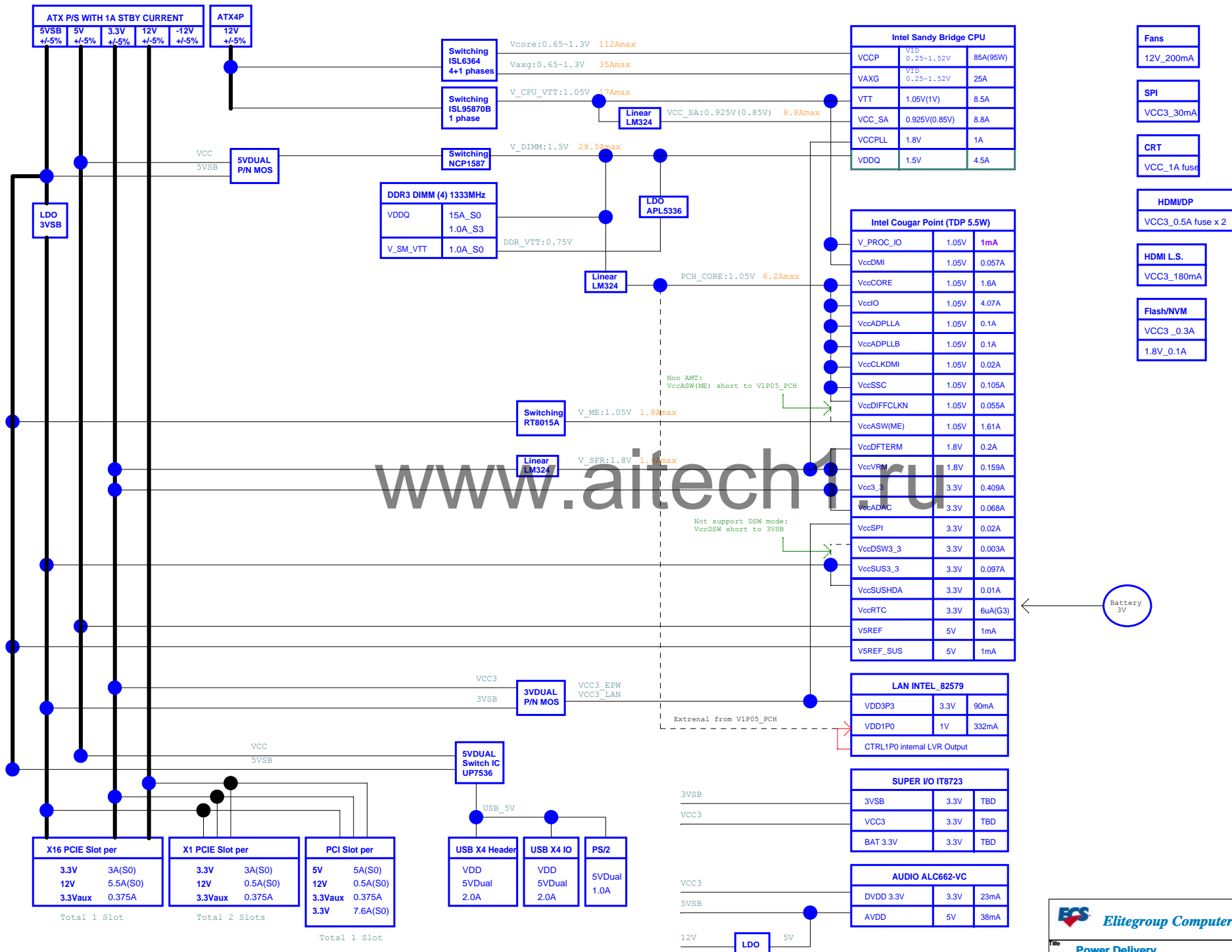
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option





Deep Sleep S5/S4 Power sequence

